PHILIPS

Data handbook

PHILIPS Electronic components and materials

Semiconductors

Book S5　　1988

Small-signal field-effect transistors

SMALL-SIGNAL FIELD-EFFECT TRANSISTORS

SELECTION GUIDE

N-channel junction field-effect transistors, general purpose

type number	envelope	RATINGS ±V_{DS} V	I_G mA	CHARACTERISTICS I_{DSS} min.-max. mA	$-V_{(P)GS}$ max. V	$|y_{fs}|$ min. f = 1 kHz mS	C_{rs} typ. pF	remarks	page
BC264A	TO-92 var.	30	10	2,0-4,5	>0,5	2,5	1,2	hi-fi amplifiers and a.f. equipment	49
BC264B				3,5-6,5		3,0			49
BC264C				5,0-8,0		3,5			49
BC264D				7,0-12,0		4,0			49
BF245A	TO-92 var.	30	10	2,0-6,5	8,0	3,0-6,5	1,1	d.c., l.f. and h.f. amp.	55
BF245B				6-15					55
BF245C				12-25					55
BF247A	TO-92 var.	25	10	30-80	0,6-14,5	8	3,5	v.h.f. and u.h.f. amp. general purpose sw.	67
BF247B				60-140					67
BF247C				110-250					67
BF256A	TO-92 var.	30	10	3-7	7,5	4,5	0,7	v.h.f. and u.h.f. appl.	69
BF256B				6-13					69
BF256C				11-18					69
BF410A	TO-92 var.	20*	10	0,7-3,0	typ. 0,8	2,5	0,3	r.f. stages f.m. portables	81
BF410B				2,5-7,0	typ. 1,5	4,0		r.f. stages car radios	81
BF410C				6-12	typ. 2,2	6,0		r.f. stages mains radios	81
BF410D				10-18	typ. 3,0	7,0		mixer stages	81
BF510	SOT-23	20	10	0,7-3,0	typ. 0,8	2,5	0,3	r.f. stages f.m. portables	85
BF511				2,5-7,0	typ. 1,5	4,0		r.f. stages car radios	85
BF512				6-12	typ. 2,2	6,0		r.f. stages mains radios	85
BF513				10-18	typ. 3,0	7,0		mixer stages	85
BFR30	SOT-23	25	5	4-10	5	1,0-4,0	0,85	low-level general purpose amplifiers	99
BFR31				1-5	2,5	1,5-4,5			99
BFR101A	SOT-143	30	10	0,2-1,5	1,0	1,2	–	source follower	109
BFR101B				1-5	2,5	2,5	–		109

* Asymmetrical.

N-channel junction field-effect transistors, general purpose

type number	envelope	RATINGS ±V_{DS} V	CHARACTERISTICS I_G mA	I_{DSS} min.-max. mA	$-V_{(P)GS}$ max. V	$|y_{fs}|$ min. f = 1 kHz mS	C_{rs} typ. pF	remarks	page
BFT46	SOT-23	25	5	0,2-1,5	1,2	1,0	0,85	general purpose ampl.	117
BFW10	TO-72	30	10	8-20	8	3,5-6,5	0,6	broad band up to 300 MHz and differential ampl.	125
BFW11				4-10	6	3,0-6,5			125
BFW12	TO-72	30	5	1-5	2,5	2,0	0,6	low current-low voltage applications	137
BFW13				0,2-1,5	1,2	1,0			137
BFW61	TO-72	25	10	2-20	8	2,0-6,5	<2,0	general purpose ampl.	147
2N3822	TO-72	50	10	2-10	6	3,0-6,5	<3,0	general purpose h.f. ampl.	173
2N3823	TO-72	30	10	4-20	8	3,5-6,5	<2,0	industrial i.f./r.f. ampl.	175

N-channel junction field-effect transistors for differential amplifiers

type	envelope	RATINGS			CHARACTERISTICS								
		individual transistor	individual transistor	total device	individual transistor				total device				
		$\pm V_{DS}$	I_G	I_G	I_{DSS}		$-V_{(P)GS}$		$\|\Delta V_{GS}\|$	$\|\dfrac{d\,\Delta V_{GS}}{dT}\|$	$\|\Delta \dfrac{1}{g_{fs}}\|$	$\|\Delta \dfrac{g_{os}}{g_{fs}}\|$	CMRR
		V	mA	mA	min. mA	max. mA	min. V	max. V	max. mV	max. μV/K	max. Ω	max. μV/V	min. dB
BFQ10	TO-71	30	—	10	0,5	10	0,5	3,5	5	5	6	10	100
BFQ11									10	5	6	30	90
BFQ12									10	10	12	30	90
BFQ13									10	20	12	30	90
BFQ14									15	20	12	30	90
BFQ15									20	40	20	30	90
BFQ16									50	50	30	100	80
BFS21	SOT-52	30	10	0,5	1	—	—	6	20	75	15	1000	60
BFS21A									10	40	7,5	500	66

page: BFQ10–BFQ16 → 91; BFS21, BFS21A → 111

N-channel junction field-effect transistors for switching

type number	envelope	RATINGS				CHARACTERISTICS						
		V_{DS} V	I_G mA	I_{DSS} min. mA	max. mA	$-V_{(P)GS}$ min. V	max. V	$r_{ds\,on}$ max. Ω	C_{rs} max. pF	t_{on} max. ns	t_{off} max. ns	page
BSR56	SOT-23	40	50	50	–	4	10	25	5	9	25	153
BSR57				20	100	2	6	40		10	50	153
BSR58				8	80	0,8	4	60		20	100	153
BSV78	TO-18	40	50	50	–	3,75	11	25	5	10	10	161
BSV79				20	–	2	7,0	40		18	16	161
BSV80				10	–	1	5,0	60		30	32	161
PMBF4391	SOT-23	40	50	50	150	4	10	30	3,5	15	20	169
PMBF4392		40		25	75	2	5	60		15	35	169
PMBF4393		40		5	30	0,5	3	100		15	50	169
2N3966	TO-72	30	10	2	–	4	6	220	1,5	120	100	177
2N4091	TO-18	40	10	30	–	5	10	30	5	25	40	181
2N4092				15	–	2	7,0	50		35	60	181
2N4093				8	–	1	5,0	80		60	80	181
2N4391	TO-18	50	50	50	150	4	10	30	3,5	15	20	185
2N4392				25	75	2	5,0	60		15	35	185
2N4393				5	30	0,5	3,0	100		15	50	185
2N4856	TO-18	40	50	50	–	4	10	25	8	9	25	189
2N4857		40		20	100	2	6	40		10	50	189
2N4858		40		8	80	0,8	4	60		20	100	189
2N4859		30		50	–	4	10	25		9	25	189
2N4860		30		20	100	2	6	40		10	50	189
2N4861		30		8	80	0,8	4	60		20	100	189

P-channel junction field-effect transistors for switching

type number	envelope	RATINGS		CHARACTERISTICS								page
		$\pm V_{DS}$ V	I_G mA	I_{DSS} min. mA	max.	$-V_{(P)GS}$ min. V	max.	$R_{ds\,on}$ max. Ω	C_{rs} max. pF	t_{on} max. ns	t_{off} max. ns	
BSJ174	TO-92	30	50	20	135	5	10	85	4	7	15	149
BSJ175				7	70	3	6	125		15	30	149
BSJ176				2	35	1	4	250		35	35	149
BSJ177				1,5	20	0,8	2,25	300		45	40	149
BSR174	SOT-23	30	50	20	135	5	10	85	4	7	15	157
BSR175				7	70	3	6	125		15	30	157
BSR176				2	35	1	4	250		35	35	157
BSR177				1,5	20	0,8	2,25	300		45	45	157

N-channel MOS-FETs single gate for switching

type number	envelope	RATINGS		CHARACTERISTICS						page
		V_{DS} V	I_D mA	I_{DSS} min. mA	$-V_{(P)GS}$** V	mode	$r_{ds\,on}$ max. Ω	C_{rs} typ. pF	t_{on}/t_{off} typ. ns	
BFR29	TO-72	30*	20	10 – 40	0,5 – 3,5	depl	–	0,4	–	195
BSD10	TO-72	10	50	–	–	depl	30	0,6	1/5	203
BSD12		20		–	2					203
BSD20	SOT-143	10	50	–	–	depl	30	0,6	1/5	207
BSD22		20		–	2					207
BSD212		10								211
BSD213	TO-72	10	50	–	0,1 – 2	enh	70	0,6	1/5	211
BSD214		20								211
BSD215		20								211
BSS83	SOT-143	10	50	–	0,1 – 2	enh	45	0,6	1/5	215
BSV81	TO-72	30*	25	–	–	depl	100	0,5	–	219

* V_{DB}/V_{SB}
** enh. types $V_{GS(th)}$

N-channel MOS-FETS, Dual gate

type number	envelope	RATINGS				CHARACTERISTICS					remarks	page
		V_{DS}	I_D	I_{DSS}		$-V_{(P)G1-S}$ max.	$\|y_{fs}\|$ $f = 1\,kHz$ min.	C_{is} typ.	C_{os} typ.	F typ.		
		V	mA	min. mA	max.	V	mS			dB		
BF960*	SOT-103	20	20	2	20	3,5	9,5	1,8	0,9	2,8	UHF	227
BF964*	SOT-103	20	30	2	20	2,5	15	2,5	1,0	1,5	VHF	231
BF964S*	SOT-103	20	50	4	20	2,5	15	2,5	1,0	1,0	VHF	235
BF965*	SOT-103	20	30	2	20	2,5	15	2,5	1,0	1,0	VHF	241
BF966*	SOT-103	20	30	2	20	2,5	15	2,2	0,8	2,8	UHF	245
BF966S*	SOT-103	20	30	4	20	2,5	15	2,3	0,8	1,8	UHF	249
BF980*	SOT-103	18	30	–	–	1,3	17	2,6	1,1	2,8	UHF	255
BF981*	SOT-103	20	20	4	25	2,5	10	2,1	1,1	1,0	VHF	259
BF982*	SOT-103	20	40	–	–	1,3	20	4,0	2,0	1,2	VHF	267
BF989*	SOT-143	20	20	2	20	2,7	9,5	1,8	0,9	2,8	UHF	271
BF990*	SOT-143	18	30	–	–	1,3	17	2,6	1,2	2,8	UHF	273
BF991*	SOT-143	20	20	4	25	2,5	10	2,1	1,1	1,0	VHF	277
BF992*	SOT-143	20	40	–	–	1,3	20	4,0	2,0	1,2	VHF	279
BF994*	SOT-143	20	30	2	20	2,5	15	2,5	1,0	1,5	VHF	281
BF994S*	SOT-143	20	50	4	20	2,5	15	2,5	1,0	1,0	VHF	285
BF996*	SOT-143	20	30	2	20	2,5	15	2,2	0,8	2,8	UHF	287
BF996S*	SOT-143	20	30	4	20	2,5	15	2,3	0,8	1,8	UHF	291
BF997*	SOT-143	20	30	2	20	2,5	15	2,5	1,0	1,0	VHF	293
BFR84*	TO-72	20	50	20	55	3,8	12	5,5	3,5	2,3	General purpose	297

* Protected against excessive input voltage surges.

N-channel vertical D-MOSFETs for switching

type number	envelope	RATINGS				CHARACTERISTICS						page
		V_{DS} V	I_D mA	P_{tot} at T_{amb} mW	°C	$V_{GS(th)}$ V	R_{DSon} typ. Ω	max. Ω	@ I_D mA	V_{GS} V	t_{on}/t_{off} max. ns	
BS107	TO-92 var.	200	120	500	25	1,8 (typ.)	15	28	20	2,6	10/10	305
BS170	TO-92 var.	60	500	830	25	0,8-3,0	2,5	5	200	10	10/10	309
BST70A	TO-92 var.	80	500	1000	25	1,5-3,5	2	4	500	10	10/15	317
BST72A	TO-92 var.	80	300	830	25	1,5-3,5	7	10	150	5	10/10	321
BST74A	TO-92 var.	200	300	1000	25	0,8-2,8	6	12	250	10	10/25	325
BST76A	TO-92 var.	180	300	1000	25	0,7-2,7	7	10	15	3	10/15	329
BST78	TO-126	450	750	15000	75*	2,0-4,0	10	14	100	10	10/100	333
BST80	SOT-89	80	500	1000	25	1,5-3,5	2	4	500	10	10/15	337
BST82	SOT-23	80	175	300	25	1,5-3,5	7	10	150	5	10/10	341
BST84	SOT-89	200	250	1000	25	0,8-2,8	6	12	250	10	10/25	345
BST86	SOT-89	180	300	1000	25	0,7-2,7	7	10	15	3	10/15	349
BST95	TO-39	200	2000	10000	25*	1-3	1,8	2	1500	10	10/25*	353
BST97	TO-18	180	300	1500	25*	0,7-2,7	7	10	15	3	10/15	357
PH6659	TO-92 var.	35	750				1,5		300	5		377
PH6660		60	500	1000	25	0,8-2,0	1,8		300	5	10/10	377
PH6661		90	500				2,4		300	5		377
2N6659	TO-39	35	1400	6250	25*	0,8-2,0	1,5	5	300	5	10/20	381
2N6660	TO-39	60	1100	6250	25*	0,8-2,0	1,8	5	300	5	10/20	381
2N6661	TO-39	90	900	6250	25*	0,8-2,0	2,4	5,3	300	5	10/20	381

* T_{mb}

P-channel vertical D-MOSFETs for switching

type number	envelope	RATINGS				CHARACTERISTICS					page
		V_{DS}	I_D	P_{tot} at T_{amb}	$V_{GS(th)}$	R_{DSon}		$@$		t_{on}/t_{off}	
						typ.	max.	I_D	V_{GS}	typ.	
		V	mA	mW	°C	V	Ω	Ω	mA	V	ns	
BS250	TO-92 var.	45	250	830	25	1-3,5	9	14	200	10	4/10	313
BST100	TO-92 var.	60	300	1000	25	1,5-3,5	4,5	6	200	10	4/20	361
BST110	TO-92 var.	50	300	830	25	1,5-3,5	7,5	10	200	10	4/20	365
BST120	SOT-89	60	300	1000	25	1,5-3,5	4,5	6	200	10	4/20	369
BST122	SOT-89	50	250	1000	25	1,5-3,5	7,5	10	200	10	4/20	373

TYPE NUMBER SURVEY

In this alphanumeric list we present all field-effect transistors mentioned in this handbook.

type number	envelope	$\pm V_{DS}$ max. V	I_{DSS} mA	application	page
BC264A			2,0 - 4,5		49
BC264B	TO-92 var.	30	3,5 - 6,5	hi-fi amplifiers and	49
BC264C			5,0 - 8,0	a.f. equipment	49
BC264D			7,0 - 12,0		49
BF245A			2,0 - 6,5		55
BF245B	TO-92 var.	30	6,0 - 15,0	d.c., l.f. and h.f. amplifiers	55
BF245C			12 - 25		55
BF247A			30 - 80		67
BF247B	TO-92 var.	25	60 - 140	v.h.f. and u.h.f. ampl. general purpose switch	67
BF247C			110 - 250		67
BF256A			3 - 7		69
BF256B	TO-92 var.	30	6 - 13	v.h.f. and u.h.f.	69
BF256C			11 - 18		69
BF410A			0,7 - 3,0	r.f. stages f.m. portables	81
BF410B	TO-92 var.	20*	2,5 - 7,0	r.f. stages car radios	81
BF410C			6 - 12	r.f. stages mains radios	81
BF410D			10 - 18	mixer stages	81
BF510			0,7 - 3,0	r.f. stage f.m. portables	85
BF511	SOT-23	20	2,5 - 7,0	r.f. stage car radios	85
BF512			6 - 12	r.f. stage mains radios	85
BF513			10 - 18	mixer stages	85
BF960	SOT-103	20	2 - 20	r.f. stage UHF TV tuner	227
BF964	SOT-103	20	2 - 20	r.f./mixer stage VHF TV tuner	231
BF964S	SOT-103	20	4 - 20	v.h.f. applications in TV tuner	235
BF965	SOT-103	20	2 - 20	v.h.f. TV tuner	241
BF966	SOT-103	20	2 - 20	r.f. stage UHF TV tuner	245
BF966S	SOT-103	20	4 - 20	v.h.f. applications	249
BF980	SOT-103	18	—	r.f. stage UHF TV tuner	255
BF981	SOT-103	20	4 - 25	r.f./mixer stage VHF TV tuner	259
BF982	SOT-103	20	—	r.f./mixer stage VHF TV tuner and FM radio tuner	267
BF989	SOT-143	20	2 - 20	u.h.f. TV tuners	271
BF990	SOT-143	18	—	u.h.f. TV tuners	273
BF991	SOT-143	20	4 - 25	v.h.f. TV and f.m. tuners	277
BF992	SOT-143	20	—	v.h.f. TV and f.m. tuners	279
BF994	SOT-143	20	2 - 20	u.h.f./v.h.f. TV tuners	281
BF994S	SOT-143	20	4 - 20	v.h.f. TV tuners	285
BF996	SOT-143	20	2 - 20	u.h.f. TV tuners	287
BF996S	SOT-143	20	4 - 20	u.h.f. TV tuners	291
BF997	SOT-143	20	2 - 20	u.h.f./v.h.f. TV tuners	293

* Asymmetrical.

** V_{DB}.

type number	envelope	$\pm V_{DS}$ max V	I_{DSS} mA	application	page
BFQ10					91
BFQ11					91
BFQ12					91
BFQ13	TO-71	30	0,5 - 10	low level differential amplifiers	91
BFQ14					91
BFQ15					91
BFQ16					91
BFR29	TO-72	30**	10 - 40	v.h.f./low leakage/low noise	195
BFR30	SOT-23	25	4 - 10	general purpose amplifiers	99
BFR31			1 - 5		99
BFR84	TO-72	20	20 - 55	general industrial	297
BFR101A	SOT-143	30	0,2 - 1,5	source follower	109
BFR101B			1,0 - 5,0		109
BFS21	SOT-52	30	> 1	low level differential amplifiers	111
BFS21A					111
BFT46	SOT-23	25	0,2 - 1,5	general purpose amplifiers	117
BFW10	TO-72	30	8 - 20	wide-band up to 300 MHz and differential amplifiers	125
BFW11			4 - 10		125
BFW12	TO-72	30	1 - 5	low current-low voltage	137
BFW13			0,2 - 1,5		137
BFW61	TO-72	25	2 - 20	general purpose	147
BS107	TO-92 var.	200	< 0,03	relay and line-transformer	305
BS170	TO-92 var.	60	< 0,5 μA	drivers	309
BS250	TO-92 var.	45	< 0,5 μA	drivers	313
BSD10	TO-72	10	—	switch/convertor/chopper	203
BSD12		20			203
BSD20	SOT-143	10	—	switch/convertor/chopper	207
BSD22		20	—		207
BSD212		10	—		211
BSD213	TO-72	10	—	switch/convertor/chopper	211
BSD214		20	—		211
BSD215		20	—		211
BSJ174			20 - 135		149
BSJ175	TO-92	30	7 - 70	switch/chopper	149
BSJ176			2 - 35		149
BSJ177			1,5 - 20		149
BSR56			> 50		153
BSR57	SOT-23	40	20 - 100	switch/chopper	153
BSR58			8 - 80		153
BSR174			20 - 135		157
BSR175	SOT-23	30	7 - 70	switch/chopper	157
BSR176			2 - 35		157
BSR177			1,5 - 20		157
BSS83	SOT-143	10	—	switch/switch driver	215

* I_{Dmax} (A).
** V_{DB}.

type number	envelope	$\pm V_{DS}$ max. V	I_{DSS} mA	application	page
BST70A	TO-92 var.	80	0,5		317
BST72A	TO-93 var.	80	0,3	high-speed relay and	321
BST74A	TO-92 var.	200	0,3	line transformer driver	325
BST76A	TO-92 var.	180	0,3	in telephone circuits	329
BST78	TO-202	450	0,75		333
BST80	SOT-89	80	0,5*		337
BST82	SOT-23	80	0,175*	relay, high-speed and	341
BST84	SOT-89	200	0,25	line-transformer drivers	345
BST86	SOT-89	180	0,3*		349
BST95	TO-39	200	$< 10{,}000$	motor control	353
BST97	TO-18	180	0,3		357
BST100	TO-92 var.	60	0,3	relay, high-speed and	361
BST110	TO-92 var.	50	0,25	line-transformer drivers	365
BST120	SOT-89	60	0,3		369
BST122	SOT-89	50	0,25		373
BSV78			> 50		161
BSV79	TO-18	40	> 20	switch	161
BSV80			> 10		161
BSV81	TO-72	30	—	switch-chopper	219
PH6659		35			377
PH6660	TO-92 var.	60	$< 10{,}000$	inverter/driver	377
PH6661		90			377
PMBF4391			> 40		169
PMBF4392	SOT-123	40	> 25	switch/chopper	169
PMBF4393			> 5		169
2N3822	TO-72	50	2-10	general purpose h.f. ampl.	173
2N3823	TO-72	30	4-20	industrial i.f./r.f. ampl.	175
2N3966	TO-72	30	> 2	low power switch	177
2N4091			> 30		181
2N4092	TO-18	40	> 15	low power switch	181
2N4093			> 8		181
2N4391			> 50		185
2N4392	TO-18	40	> 25	low power switch/chopper	185
2N4393			> 5		185
2N4856		40	> 50		189
2N4857		40	> 20		189
2N4858		40	> 8		189
2N4859	TO-18	30	> 50	low power switch/chopper	189
2N4860		30	> 20		189
2N4861		30	> 8		189
2N6659		35	1,4*		381
2N6660	TO-39	60	1,1*	H.F. inverters and line drivers	381
2N6661		90	0,9*		381

* I_{Dmax} (A).

GENERAL

PRO ELECTRON TYPE DESIGNATION CODE
FOR SEMICONDUCTOR DEVICES

This type designation code applies to discrete semiconductor devices — as opposed to integrated circuits —, multiples of such devices and semiconductor chips.

"Although not all type numbers accord with the Pro Electron system, the following explanation is given for the ones that do."

A basic type number consists of:

TWO LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST LETTER

The first letter gives information about the material used for the active part of the devices.

A. GERMANIUM or other material with band gap of 0,6 to 1,0 eV.
B. SILICON or other material with band gap of 1,0 to 1,3 eV.
C. GALLIUM-ARSENIDE or other material with band gap of 1,3 eV or more.
R. COMPOUND MATERIALS (e.g. Cadmium-Sulphide).

SECOND LETTER

The second letter indicates the function for which the device is primarily designed.

A. DIODE; signal, low power
B. DIODE; variable capacitance
C. TRANSISTOR; low power, audio frequency ($R_{th\,j-mb} > 15$ K/W)
D. TRANSISTOR; power, audio frequency ($R_{th\,j-mb} \leqslant 15$ K/W)
E. DIODE; tunnel
F. TRANSISTOR; low power, high frequency ($R_{th\,j-mb} > 15$ K/W)
G. MULTIPLE OF DISSIMILAR DEVICES — MISCELLANEOUS; e.g. oscillator
H. DIODE; magnetic sensitive
L. TRANSISTOR; power, high frequency ($R_{th\,j-mb} \leqslant 15$ K/W)
N. PHOTO-COUPLER
P. RADIATION DETECTOR; e.g. high sensitivity phototransistor
Q. RADIATION GENERATOR; e.g. light-emitting diode (LED)
R. CONTROL AND SWITCHING DEVICE; e.g. thyristor, low power ($R_{th\,j-mb} > 15$ K/W)
S. TRANSISTOR; low power, switching ($R_{th\,j-mb} > 15$ K/W)
T. CONTROL AND SWITCHING DEVICE; e.g. thyristor, power ($R_{th\,j-mb} \leqslant 15$ K/W)
U. TRANSISTOR; power, switching ($R_{th\,j-mb} \leqslant 15$ K/W)
X. DIODE: multiplier, e.g. varactor, step recovery
Y. DIODE; rectifying, booster
Z. DIODE; voltage reference or regulator (transient suppressor diode, with third letter **W**)

SERIAL NUMBER

Three figures, running from 100 to 999, for devices primarily intended for consumer equipment.*
One letter (Z, Y, X, etc.) and two figures, running from 10 to 99, for devices primarily intended for industrial/professional equipment.*
This letter has no fixed meaning except W, which is used for transient suppressor diodes.

VERSION LETTER

It indicates a minor variant of the basic type either electrically or mechanically. The letter never has a fixed meaning, except letter R, indicating reverse voltage, e.g. collector to case or anode to stud.

SUFFIX

Sub-classification can be used for devices supplied in a wide range of variants called associated types.
Following sub-coding suffixes are in use:

1. VOLTAGE REFERENCE and VOLTAGE REGULATOR DIODES: *ONE LETTER and ONE NUMBER*
   The LETTER indicates the nominal tolerance of the Zener (regulation, working or reference) voltage
   A.   1% (according to IEC 63: series E96)
   B.   2% (according to IEC 63: series E48)
   C.   5% (according to IEC 63: series E24)
   D. 10% (according to IEC 63: series E12)
   E. 20% (according to IEC 63: series E6)
   The number denotes the typical operating (Zener) voltage related to the nominal current rating for the whole range.
   The letter 'V' is used instead of the decimal point.

2. TRANSIENT SUPPRESSOR DIODES: *ONE NUMBER*
   The NUMBER indicates the maximum recommended continuous reversed (stand-off) voltage V_R. The letter 'V' is used as above.

3. CONVENTIONAL and CONTROLLED AVALANCHE RECTIFIER DIODES and THYRISTORS: *ONE NUMBER*
   The NUMBER indicates the rated maximum repetitive peak reverse voltage (V_{RRM}) or the rated repetitive peak off-state voltage (V_{DRM}), whichever is the lower. Reversed polarity is indicated by letter R, immediately after the number.

4. RADIATION DETECTORS: *ONE NUMBER,* preceded by a hyphen (–)
   The NUMBER indicates the depletion layer in μm. The resolution is indicated by a version LETTER.

5. ARRAY OF RADIATION DETECTORS and GENERATORS: *ONE NUMBER,* preceded by a stroke (/).
   The NUMBER indicates how many basic devices are assembled into the array.

* When these serial numbers are exhausted the serial number for consumer types may be extended to four figures, and that for industrial types to three figures.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

SCATTERING PARAMETERS

In distinction to the conventional h, y and z-parameters, s-parameters relate to travelling wave conditions. The figure below shows a two-port network with the incident and reflected waves a_1, b_1, a_2 and b_2.

$$a_1 = \frac{V_{i1}}{\sqrt{Z_0}} \qquad\qquad a_2 = \frac{V_{i2}}{\sqrt{Z_0}}$$

$$b_1 = \frac{V_{r1}}{\sqrt{Z_0}} \qquad\qquad b_2 = \frac{V_{r2}}{\sqrt{Z_0}}$$

[1])
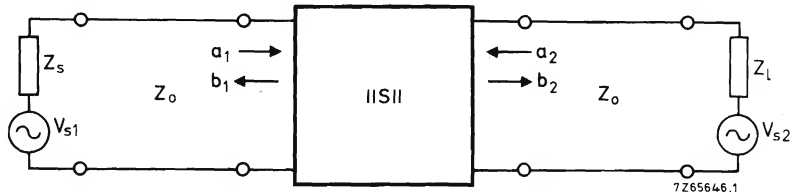
Z_0 = characteristic impedance of the transmission line in which the two-port is connected.

V_i = incident voltage

V_r = reflected (generated) voltage

The four-pole equations for s-parameters are:

$$b_1 = s_{11}a_1 + s_{12}a_2$$
$$b_2 = s_{21}a_1 + s_{22}a_2$$

Using the subscripts i for 11, r for 12, f for 21 and o for 22, it follows that:

$$s_i = s_{11} = \frac{b_1}{a_1}\bigg|_{a_2 = 0}$$

$$s_r = s_{12} = \frac{b_1}{a_2}\bigg|_{a_1 = 0}$$

$$s_f = s_{21} = \frac{b_2}{a_1}\bigg|_{a_2 = 0}$$

$$s_o = s_{22} = \frac{b_2}{a_2}\bigg|_{a_1 = 0}$$

[1]) The squares of these quantities have the dimension of power.

The s-parameters can be named and expressed as follows:

$s_i = s_{11}$ = Input reflection coefficient.

The complex ratio of the reflected wave and the incident wave at the input, under the conditions $Z_1 = Z_0 = 50\ \Omega$ and $V_{s2} = 0$.

$s_r = s_{12}$ = Reverse transmission coefficient.

The complex ratio of the generated wave at the input and the incident wave at the output, under the conditions $Z_S = Z_0 = 50\ \Omega$ and $V_{s1} = 0$.

$s_f = s_{21}$ = Forward transmission coefficient.

The complex ratio of the generated wave at the output and the incident wave at the input, under the conditions $Z_1 = Z_0 = 50\ \Omega$ and $V_{s2} = 0$.

$s_0 = s_{22}$ = Output reflection coefficient.

The complex ratio of the reflected wave and the incident wave at the output, under the conditions $Z_S = Z_0 = 50\ \Omega$ and $V_{s1} = 0$.

TO-92 VARIANT TRANSISTORS ON TAPE

MECHANICAL DATA

Dimensions in mm

Fig. 1 (see table below).
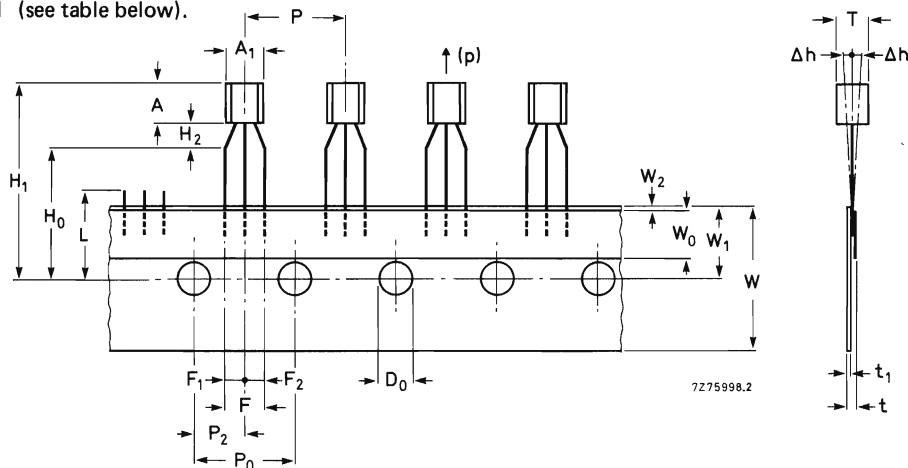
Item	Symbol	Specifications				Remarks
		min.	nom.	max.	tol.	
Body width	A_1	4,0		4,8		
Body height	A	4,8		5,2		
Body thickness	T	3,9		4,2		
Pitch of component	P		12,7		± 1	
Feed hole pitch	P_0		12,7		± 0,3	Cumulative pitch error 1,0 mm/20 pitch
Feed hole centre to component centre	P_2		6,35		± 0,4	To be measured at bottom of clinch
Distance between outer leads	F		5,08		+ 0,6 −0,2	
Component alignment	Δh		0	1		At top of body
Tape width	W		18		± 0,5	
Hold-down tape width	W_0		6		± 0,2	
Hole position	W_1		9		+ 0,7 −0,5	
Hold-down tape position	W_2		0,5		± 0,2	
Lead wire clinch height	H_0		16		± 0,5	
Component height	H_1			32,25		
Length of snipped leads	L			11,0		
Feed hole diameter	D_0		4		± 0,2	
Total tape thickness	t			1,2		t_1 0,3-0,6
Lead-to-lead distance	F_1, F_2		2,54		+ 0,4 −0,1	
Clinch height	H_2			3		
Pull-out force	(p)	6N				

PACKING

The transistors are supplied on tape in boxes (ammopack) or on reels. The number per reel is 1600 and per ammobox 2000*.

⁽¹⁾ packing label
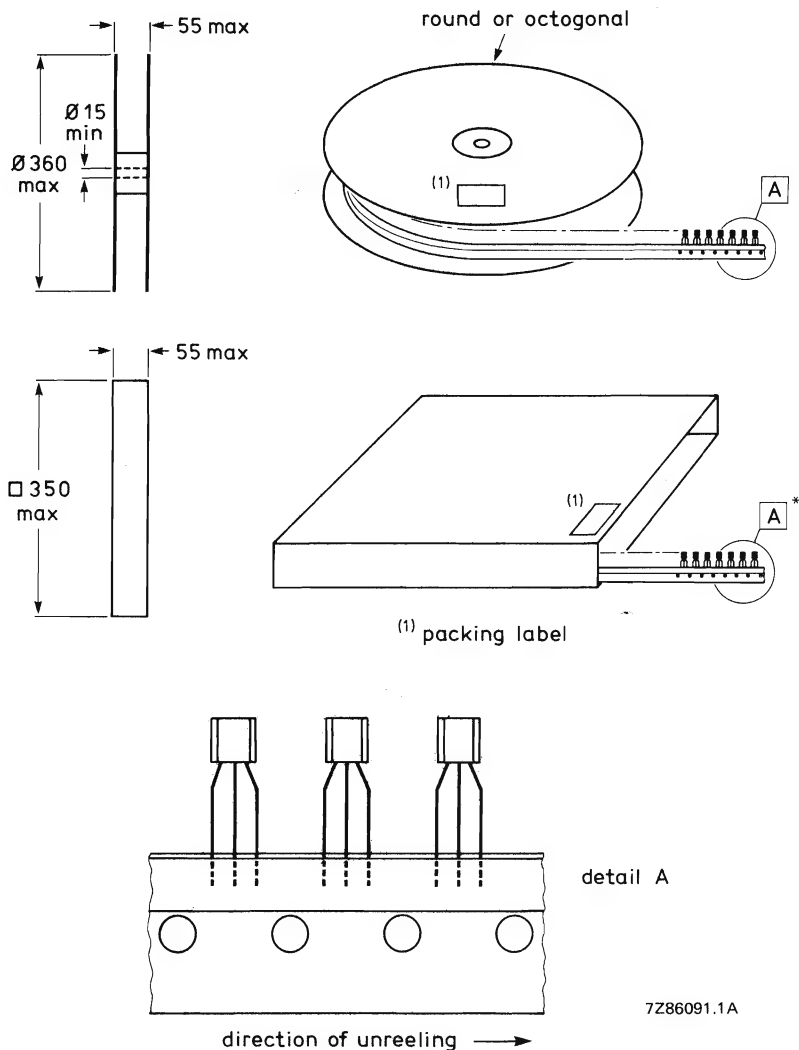
Fig. 2 Dimensions (in mm) of reel and box.

DROPOUTS

A maximum of 0,5% of the specified number of transistors in each packing may be missing. Up to 3 consecutive components may be missing provided the gap is followed by 6 consecutive components.

TAPE SPLICING

Slice the carrier tape on the back and/or front so that the feed hole pitch (P_0) is maintained (see Fig. 3).
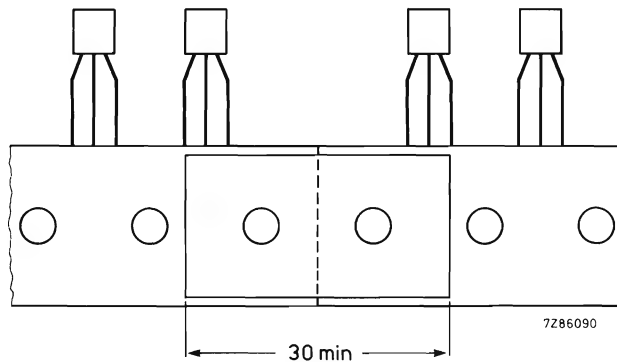
Fig. 3 Jointing tape with splicing patch.

* The ammobox has 80 layers of 25 transistors each.
Each layer contains 25 transistors plus one empty position in order to fold the layer correctly.

The ammobox is accessible from both sides enabling the user to choose between "normal"
(see Fig. 2) and "reverse" tape.

TAPE AND REEL SPECIFICATION

Semiconductors in SOT-23, SOT-143 and SOT-89 encapsulations can be delivered in reel packing for aotomatic placement on hybrid circuits and printed circuit boards. The devices are placed with the mounting side downwards in compartments.

A separate reel packing for SOT-89 encapsulation is given in Fig. 3.

direction of unreeling

7Z85817.2

Fig. 1 Configuration of bandolier. Dimensions in mm.

Compartment			tol.
length	A_0 component length		+0,2
width	B_0 component width		+0,2
depth	K_0	0,95	+0,2
width outside	B_1	3,3	max.
pitch	P	4,0	±0,1
deviation	Θ	15°	max.
hole diameter	D_1	1	min.
Sprocket hole			
diameter	D_0	1,5	+0,1
pitch	P_0	4,0	±0,1
distance	E	1,75	±0,1
cumulative (10)			
pitch error		±0,1	

Centre line dimensions			tol.
length direction	P_2	2,0	±0,05
width direction	F	3,5	±0,05
Fixing tape			
width	W_1	5,5	±0,25
thickness	–	0,1	max.
Carrier tape			
width	W	8,0	±0,2
bending	δ	0,3	max.
thickness	t	0,4	max.
Overall thickness	K	1,5	max.

Fig. 2 Configuration of reel and flange (dimensions in mm).

Flange			tol.	Hub			tol.
diameter	A	180	+0 −2	diameter	B	62	± 1,5
thickness	t	1,5	+0,5 −0,1	spindle hole	C	12,75	+0,15 −0
space between flanges	W	9,5	± 0,5	key slit			
				width	E	2	± 0,5
				depth	U	4	± 0,5
				location	O	120	degrees

Amount of devices per reel

The bandolier of a 180 mm reel contains at least 3000 devices with no more than 15 empty compartments (0,5%). Three consecutive empty places might be found provided this gap is followed by 6 consecutive devices.

The carrier tape (leader) starts with at least 75 empty positions (equivalent to 300 mm); the covering foil is at least 300 mm. In order to fix the carrier tape a self-adhesive tape of 20 to 50 mm is applied.

At the end of the bandolier (trailer) at least 75 empty positions (equivalent to a length of 300 mm) and 300 mm foil. For fixing onto the reel a self-adhesive tape of 20 to 50 mm is applied.

Semiconductors in SOT-89 encapsulations can also be delivered in reel packing for automatic placement on hybrid circuits and printed circuit boards. The devices are placed with the mounting side downwards in compartments.Total number of devices per reel is 1000.
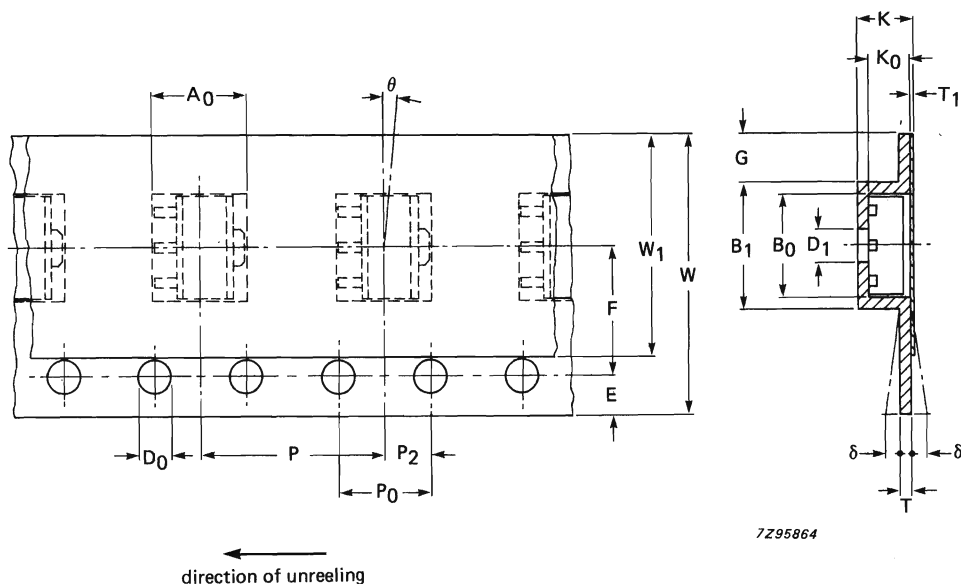
direction of unreeling

7Z95864

Fig. 3 Configuration of bandolier. Dimensions in mm.

Compartment			tol.
length	A_0 component length		
width	B_0 component width		
depth	K_0 component depth		
width outside	B_1	5,7	max.
pitch	P	8,0	± 0,1
deviation	Θ	± 5°	max.
hole diam.	D_1	1,5	min.
Sprocket hole			
diameter	D_0	1,5	+ 0,1
pitch	P_0	4,0	± 0,1
distance	E	1,75	± 0,1
cumulative (10) pitch error		± 0,1	

Centre line dimensions			tol.
length direction	P_2	2,0	± 0,05
width direction	F	5,5	± 0,1
Fixing tape			
width	W_1	9,5	max.
thickness	T_1	0,1	max.
Carrier tape			
width	W	12	± 0,2
bending	δ	0,3	max.
thickness	T	0,4	max.
Overall thickness	K	2,4	max.
distance	G	1,8	min.

SOLDERING RECOMMENDATIONS
SOT-23, SOT-143 AND SOT-89 ENVELOPES

SOT-23, SOT-143 and SOT-89 devices are ideally suited for placement onto thick and thin film substrates and printed circuit boards.

To assure reliable and consistent connections particular attention should be paid to:

1. **Flux**

   A non-active flux is recommended. Where active fluxes are employed, great care in subsequent substrate cleaning must be exercised.

2. **Metal-alloy solder or solder paste**

   Correct choice of solder alloy or solder paste to be employed e.g. 62% Sn, 36% Pb, 2% Ag or 60% Sn/40% Pb. Any paste used should contain at least 85% metal dry weight.

3. **Soldering temperature**

   This will vary according to the actual method employed.

REFLOW SOLDERING

The preferred technique for mounting microminiature components on hybrid thick and thin-film is the method of reflow soldering.

The tags of SOT-23, SOT-143 and SOT-89 envelopes are pre-tinned and the best results are obtained if a similar solder is applied to the corresponding soldering areas on the substrate. This can be done by either dipping the substrate in a solder bath or by screen printing a solder paste.

The maximum temperature of the leads or tab during the soldering cycle should not exceed 285 °C. The most economic method of soldering is a process in which all different components are soldered simultaneously for example SOT-23, SOT-143 or SOT-89 devices, capacitors and resistors.

Having first been fluxed, all components are positioned on the substrate. The slight adhesive force of the flux is sufficient to keep the components in place. Solder paste contains a flux and has therefore good inherent adhesive properties which eases positioning of the components.

With the components in position the substrate is heated to a point where the solder begins to flow. This can be done on a heating plate or on a conveyor belt running through an infrared tunnel. The maximum allowed temperature of the plastic body of a device must be kept below 280 °C during the soldering cycle. For further temperature behaviour during the soldering process see Figs 2 and 3.

The surface tension of the liquid solder tends to draw the tags of the device towards the centre of the soldering area and has thus a correcting effect on slight mispositionings. However, if the layout leaves something to be desired the same effect can result in undesirable shifts; particularly if the soldering areas on the substrate and the components are not concentrally arranged. This problem can be solved using a standard contact pattern, which leaves sufficient scope for the self-positioning effect (see Figs 4 and 5).

After cooling the connections may be visually inspected and, where necessary, repaired with a light soldering iron. Finally any remaining flux must be removed carefully.

WAVE SOLDERING

The normal (dual) wave soldering process can also be aplied to SOT-23 and SOT-143 envelopes We do not recommend SOT-89 for wave soldering.

IMMERSION SOLDERING

Where a complete substrate or printed circuit board is immersed in solder:
a. The temperature of the soldering bath should not exceed 280 °C.
b. The duration of the soldering cycle should not exceed 10 seconds.
c. Forced cooling may be applied (see Fig. 1).

HAND SOLDERING

It is possible to solder microminiature devices with a light hand-held soldering iron, but this method has obvious drawbacks and should therefore be restricted to laboratory use and/or incidental repairs on production circuits.

1. It is time-consuming and expensive.

2. The device cannot be positioned accurately and therefore the connecting tags may come into contact with the substrate and damage it.

3. There is a great risk of breaking either substrate or even internal connections inside the encapsulation.

4. The envelope may be damaged by the iron.

7Z82785
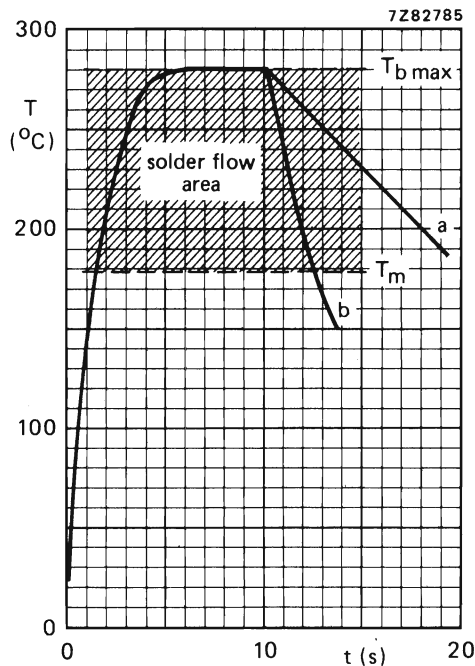
Fig. 1 Device temperature during *immersion* soldering.

Maximum time of immersion in soldering bath is 10 seconds at an ambient temperature of 25 °C.
a   = free convection cooling; b = forced cooling.
$T_{b\ max}$ = maximum bath temperature (280 °C).
T_m = melting temperature of solder (179 °C).

Fig. 2 Reflow soldering without preheating.
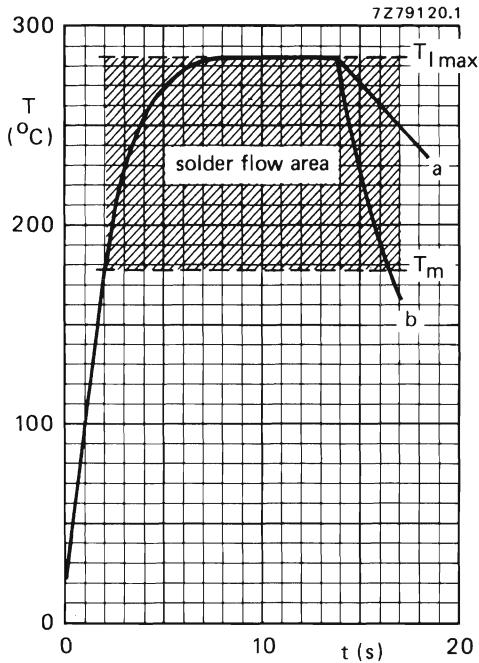
a   = free convection cooling.

b   = permissible forced cooling.

$T_{l\,max}$ = Maximum lead or tab temperature = 285 °C.

T_m = Melting point of the solder is 179 °C.

T_{amb} = 25 °C.

Time of heat supply:
without preheating max. 14 s
with preheating max. 10 s

Maximum time of preheating 45 s
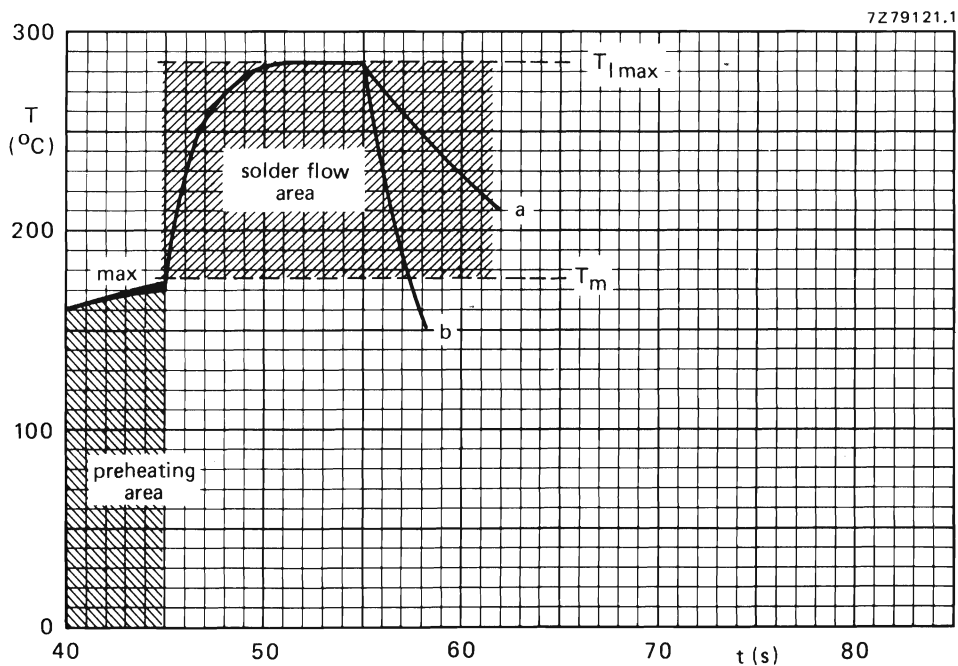
Fig. 3 Reflow soldering with preheating.

Minimum required dimensions of metal
connection pads on hybrid thick and thin-film
substrates.

Dimensions in mm
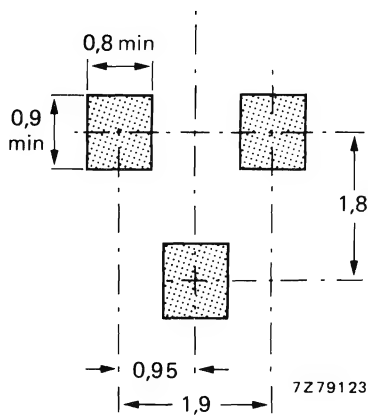
Fig. 4 SOT-23 pattern.
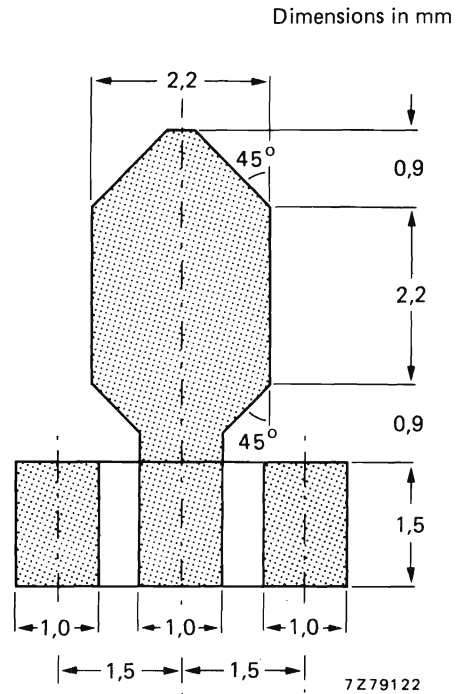
Fig. 5 SOT-89 pattern.
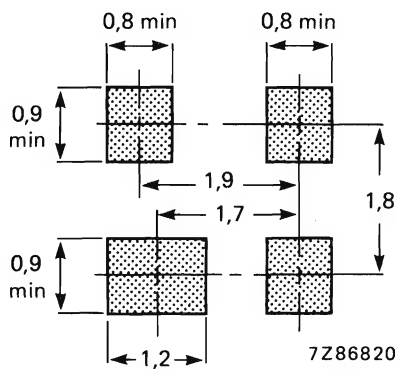
Fig. 6 SOT-143 pattern.

SOLDERING RECOMMENDATIONS SOT-103

Transistors in SOT-103 envelopes may be mounted with leads flat (Fig. 1) or bent (Figs 2 and 3). Different soldering procedures apply for the different styles of mounting.

FLAT-LEAD MOUNTING

Soldering by hand

Avoid putting any force on the leads during or just after soldering.

Solder the four leads one at a time, *not* simultaneously.

Proceed from one lead to the adjacent lead, *not* to the opposite one.

BENT-LEAD MOUNTING

If leads are bent, all four may be soldered simultaneously if desired.

DIP OR WAVE SOLDERING

When dip or wave soldering, the maximum allowable temperature of the solder is 260 °C. This temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds. The device may be mounted up to the lead projections, but the temperature of the body must not exceed the specified storage maximum.

7Z58790.2

Fig. 1
Solder temperature   max.   300 °C
Soldering time   max.   5 s
Solder-to-case distance   min.   2 mm

7Z58791.1

Fig. 2
Solder temperature   max.   300 °C
Soldering time   max.   10 s

7Z77413
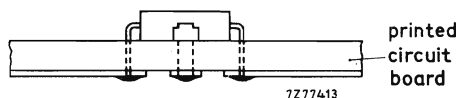
Fig. 3
Solder temperature   max.   260 °C
Soldering time   max.   5 s

THERMAL CHARACTERISTICS
OF SOT-23 AND SOT-143 ENVELOPES

The heat generated in a semiconductor chip normally flows by various paths to the surroundings (ambient).
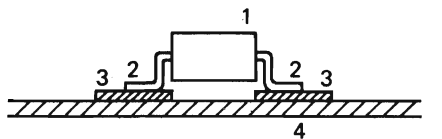
Fig. 1.

.7Z89072.A

1. Heat radiation from the envelope to ambient (1).
   This heat transfer can be neglected when the envelope is mounted on a substrate or printed circuit board.
2. Heat transmission via leads (2) soldering points (3) and substrate (4).
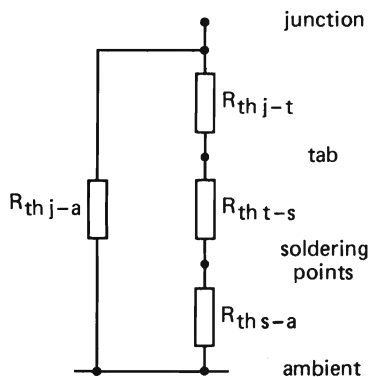
7Z89073

Fig. 2 Thermal behaviour of heat flow when the device is mounted on a substrate or printed circuit board.

$R_{th\ j\text{-}t}$ = Thermal resistance from junction to tab.

$R_{th\ t\text{-}s}$ = Thermal resistance from tab to soldering points.

$R_{th\ s\text{-}a}$ = Thermal resistance from soldering points to ambient.

$R_{th\ j\text{-}a}$ = Thermal resistance from junction to ambient.

Heat transfer directly from envelope to ambient

This depends on the difference between the temperatures of envelope and the surroundings. When the device is mounted on a substrate or printed circuit board direct heat flow can usually be neglected in relation to the heat flow via leads and substrate.

Thus the thermal model can be as in Fig. 3.

7Z89077
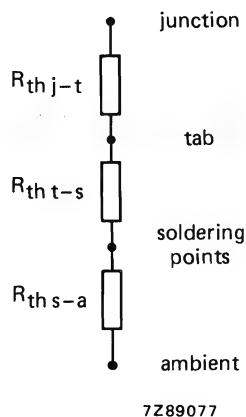
Fig. 3 Basic thermal model.

Heat transfer from junction to tab

This is an internal heat transfer and has been measured. In general it is:

for high-frequency transistors, low-power diodes and (MOS) FETs	60 K/W
for low-frequency and switching transistors	50 K/W
for low-frequency medium-power transistors	30 K/W

Heat transfer from tab to soldering points

This value has also been measured for SOT-23 with $P_{tot} < 350$ mW	280 K/W
for types of semiconductors in this envelope with $P_{tot} < 425$ mW	260 K/W
for types of semiconductors in a SOT-143 envelope this value is	310 K/W

Heat transfer from soldering points to ambient

This depends on the shape and material of tracks and substrate. In figures 4 and 5 standard mounting conditions are given to set up the maximum power ratings for SOT-23 and SOT-143 encapsulations.
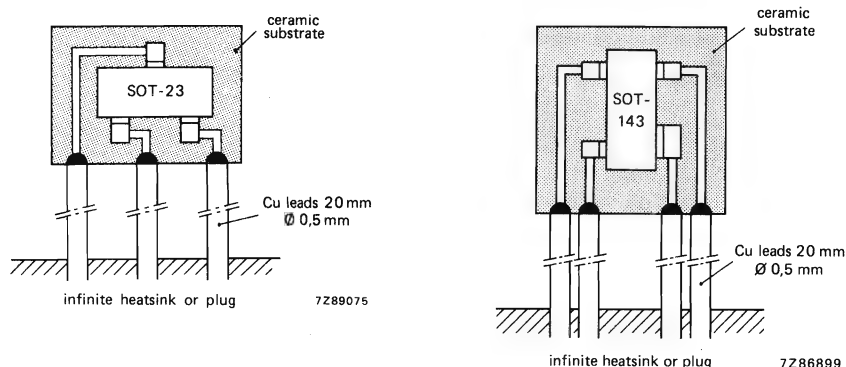
Fig. 4 Test circuits SOT-23 and SOT-143 mounting conditions on a ceramic substrate.
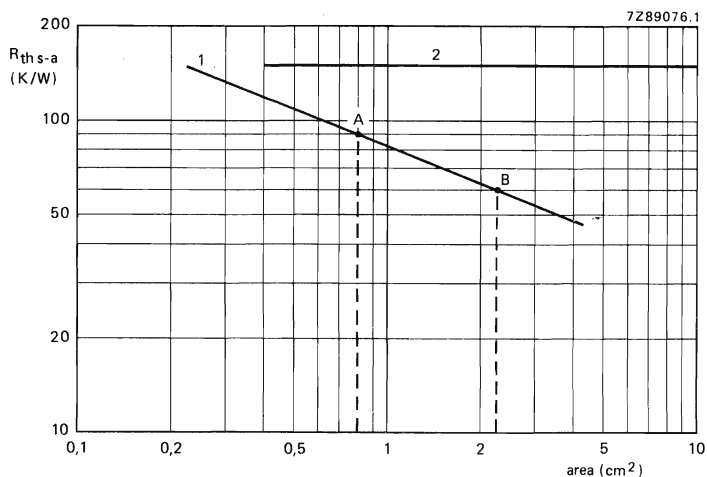
Fig. 5 Heat transfer from soldering points to ambient.

1. Ceramic substrate

Point A on the curve in Fig. 5 is for an area of the ceramic substrate of 8 mm x 10 mm x 0,7 mm for the maximum rating of all high-frequency, low-frequency and switching transistors and also for all diodes.
Point B on the curve in Fig. 5 is for an area of the ceramic substrate of 15 mm x 15 mm x 0,7 mm for the maximum rating of low-frequency medium-power semiconductors.

2. Printed circuit board

$R_{th \, s-a}$ = 150 K/W for SOT-23 and SOT-143 envelopes mounted on a printed circuit board.

The values for the thermal resistance from junction to tab, and tab to soldering points, are mentioned on page 2 and Fig. 5.

The formula for devices in SOT-23 with one crystal can be generalized:

$$T_j = P \left(R_{th\ j\text{-}t} + R_{th\ t\text{-}s} + R_{th\ s\text{-}a} \right) + T_{amb}$$
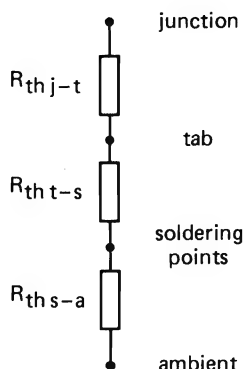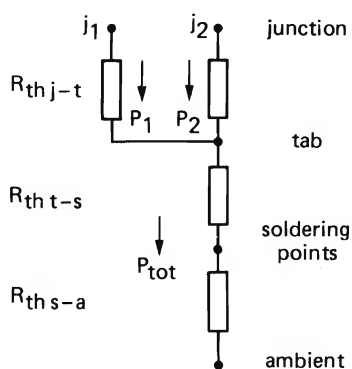
Fig. 6 Thermal model of SOT-23 envelopes with one crystal.

Fig. 7 Thermal model of SOT-23 envelopes with two crystals (double diode).

The formulae for devices with two crystals (double diodes) are:

$$T_{tab} = P_{tot} \cdot \left(R_{th\ t\text{-}s} + R_{th\ s\text{-}a} \right) + T_{amb} = P_{tot} \left(280 + 90 \right) + T_{amb}$$

$$T_{j1} = \left(P_1 \times R_{th\ j\text{-}t} \right) + T_{tab} = P_1 \cdot 60 + T_{tab}$$

$$T_{j2} = \left(P_2 \times R_{th\ j\text{-}t} \right) + T_{tab} = P_2 \cdot 60 + T_{tab}$$

As mentioned on page 2:

$R_{th\ j\text{-}t}$ for diodes is 60 K/W.

$R_{th\ s\text{-}a}$ (area 8 mm x 10 mm x 0,7 mm) = 90 K/W.

$R_{th\ t\text{-}s}$ for all semiconductors in SOT-23 = 280 K/W.

Thus:

$$T_{j1} = 60\,P_1 + 370\,P_{tot} + T_{amb}.$$

$$T_{j2} = 60\,P_2 + 370\,P_{tot} + T_{amb}.$$

DEVICE DATA

J-FETS

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for hi-fi amplifiers and other audio-frequency equipment.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	300	mW
Junction temperature	T_j	max.	150	^oC
Drain current $V_{DS} = 15\ V; V_{GS} = 0$	I_{DSS}		2 to 12	mA
Transfer admittance (common source) $V_{DS} = 15\ V; V_{GS} = 0; f = 1\ kHz$	$\lvert Y_{fs} \rvert$	typ.	3,5	mS
Noise figure at $V_{DS} = 15\ V; V_{GS} = 0$ $f = 1\ kHz; R_G = 1\ M\Omega$	F	$<$	2	dB

MECHANICAL DATA   Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:
1 = drain
2 = source
3 = gate

diameter within 2,5 max
is uncontrolled

7Z70994.2

Note: Drain and source are interchangeable

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Gate current	I_G	max.	10	mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	300	mW
Storage temperature	T_{stg}		−65 to +150	^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to ambient in free air $R_{th\ j-a}$ =   **420**   K/W

CHARACTERISTICS

T_j = 25 ^{O}C unless otherwise specified

			BC264A	B	C	D	
Gate cut-off current							
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	10	10	10	10	nA
Drain current [1])							
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	2,0	3,5	5,0	7,0	mA
		<	4,5	6,5	8,0	12,0	mA
Gate-source breakdown voltage							
$-I_G$ = 1 µA; V_{DS} = 0	$-V_{(BR)GSS}$	>	30	30	30	30	V
Gate-source voltage							
I_D = 200 µA ; V_{DS} = 15 V	$-V_{GS}$	>	0,4	0,4	0,4	0,4	V
I_D = 1,0 mA; V_{DS} = 15 V	$-V_{GS}$	>	0,2	–	–	–	V
		<	1,2	–	–	–	V
I_D = 1,5 mA; V_{DS} = 15 V	$-V_{GS}$	>	–	0,4	–	–	V
		<	–	1,4	–	–	V
I_D = 2,5 mA; V_{DS} = 15 V	$-V_{GS}$	>	–	–	0,5	–	V
		<	–	–	1,5	–	V
I_D = 3,5 mA; V_{DS} = 15 V	$-V_{GS}$	>	–	–	–	0,6	V
		<	–	–	–	1,6	V
Gate-source cut-off voltage							
I_D = 10 nA ; V_{DS} = 15 V	$-V_{(P)GS}$	>	0,5	0,5	0,5	0,5	V
y-parameters at T_{amb} = 25 ^{O}C							
V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz							
Transfer admittance	$\|y_{fs}\|$	>	2,5	3,0	3,5	4,0	mS

V_{DS} = 15 V; $-V_{GS}$ = 1 V; f = 1 MHz				
Input capacitance	C_{is}	typ.	4.0	pF
Feedback capacitance	C_{rs}	typ.	1,2	pF
Output capacitance	C_{os}	typ.	1,6	pF
Noise figure at f = 1 kHz; R_G = 1 MΩ				
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 ^{O}C	F	typ.	0,5	dB
		<	2	dB
Equivalent noise voltage at T_{amb} = 25 ^{O}C				
V_{DS} = 15 V; V_{GS} = 0; f = 10 Hz	$V_n/\sqrt{B}$	typ.	40	nV/$\sqrt{Hz}$

[1]) Measured under pulse conditions.
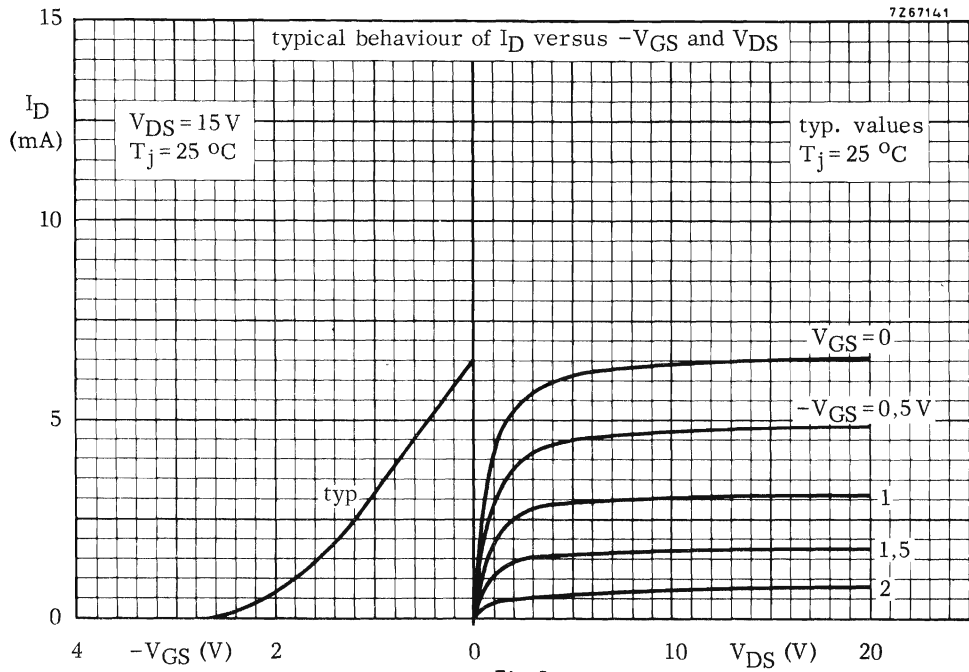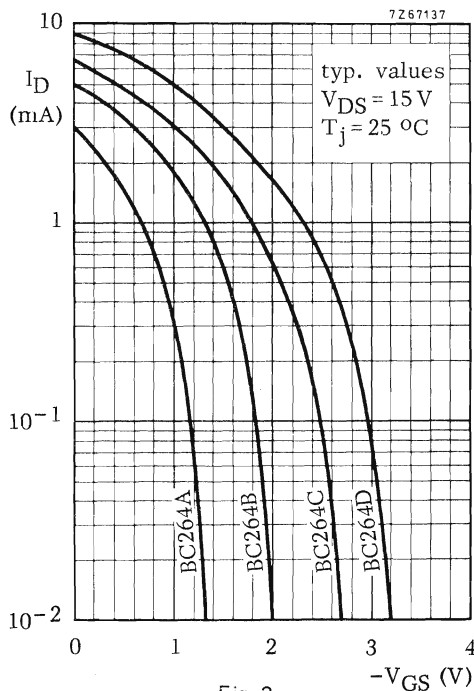
typical behaviour of I_D versus $-V_{GS}$ and V_{DS}

Fig. 2

Fig. 3

Fig. 4

7Z67138

$|Y_{fs}|$ (mA/V)

typ. values
$V_{DS} = 15\,V$
$f = 1\,kHz$
$T_{amb} = 25\,^oC$

BC264A
BC264B
BC264C
BC264D

I_D (mA)

Fig. 5

7Z67134

C_{is} (pF)

$V_{DS} = 15\,V$
$f = 1\,MHz$
$T_{amb} = 25\,^oC$

typ

$-V_{GS}$ (V)

Fig. 6

7Z67135

C_{rs}
C_{os}
(pF)

typ. values
$-V_{GS} = 2\,V$
$f = 1\,MHz$
$T_{amb} = 25\,^oC$

C_{os}

C_{rs}

V_{DS} (V)

Fig. 7

7Z67140

F (dB)

$V_{DS} = 15 \, V$
$I_D = 1 \, mA$
$f = 1 \, kHz$
$T_{amb} = 25 \, °C$

typ

Fig. 8

$R_G \, (k\Omega)$

7Z67139.1

F (dB)

$R_G = 1 \, k\Omega$

typ. values
$V_{DS} = 15 \, V$
$-V_{GS} = 1 \, V$
$T_{amb} = 25 \, °C$

$10 \, k\Omega$

$1 \, M\Omega$

Fig. 9

f (Hz)
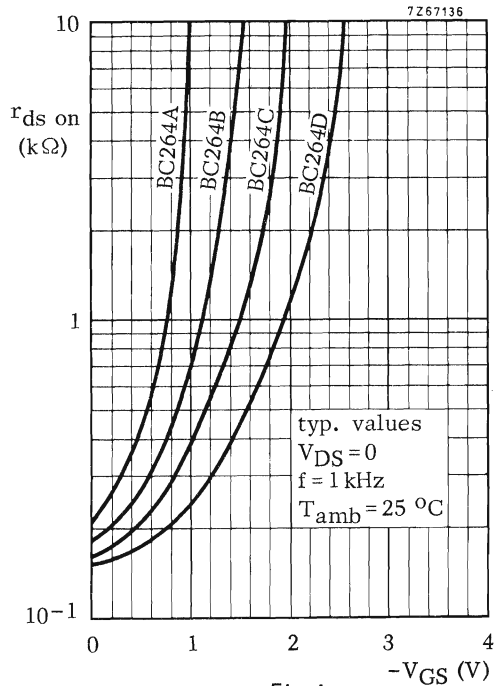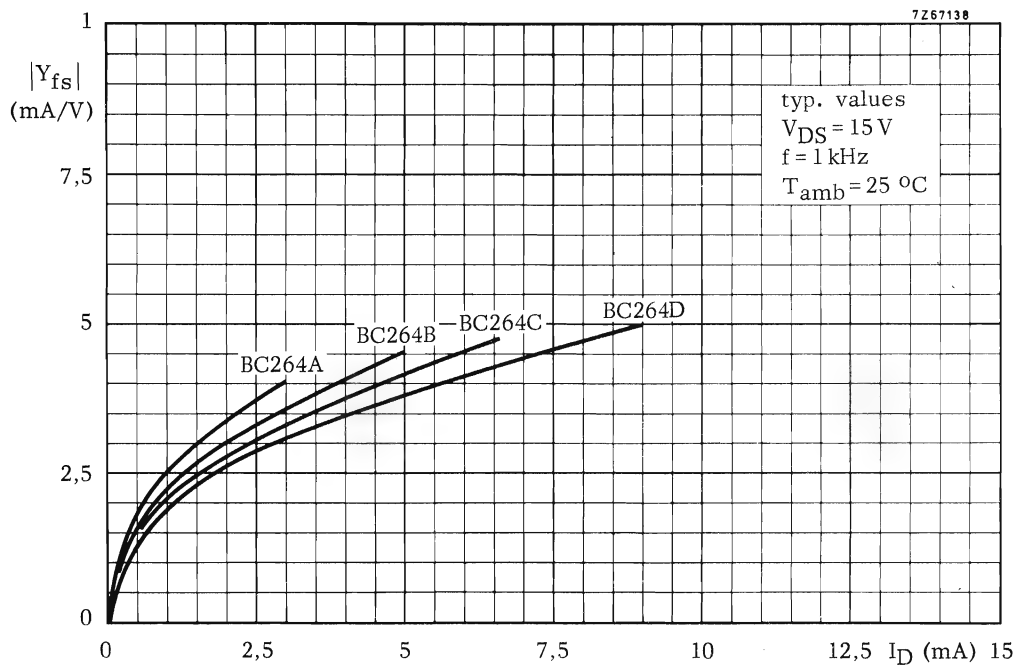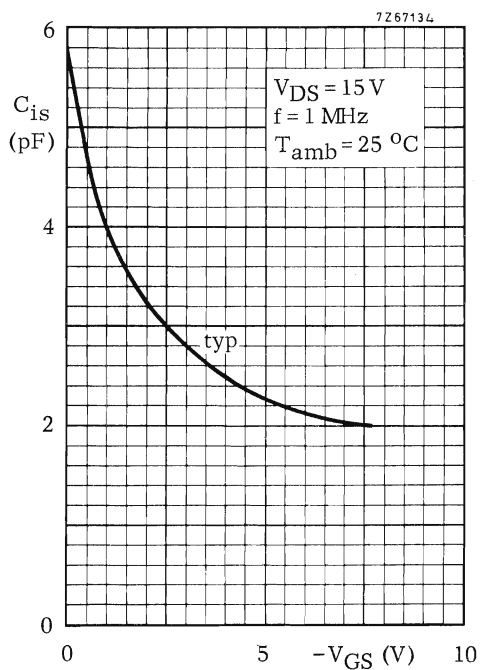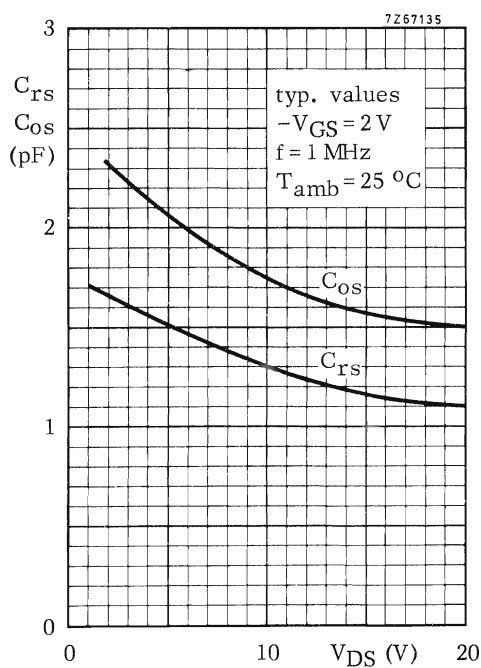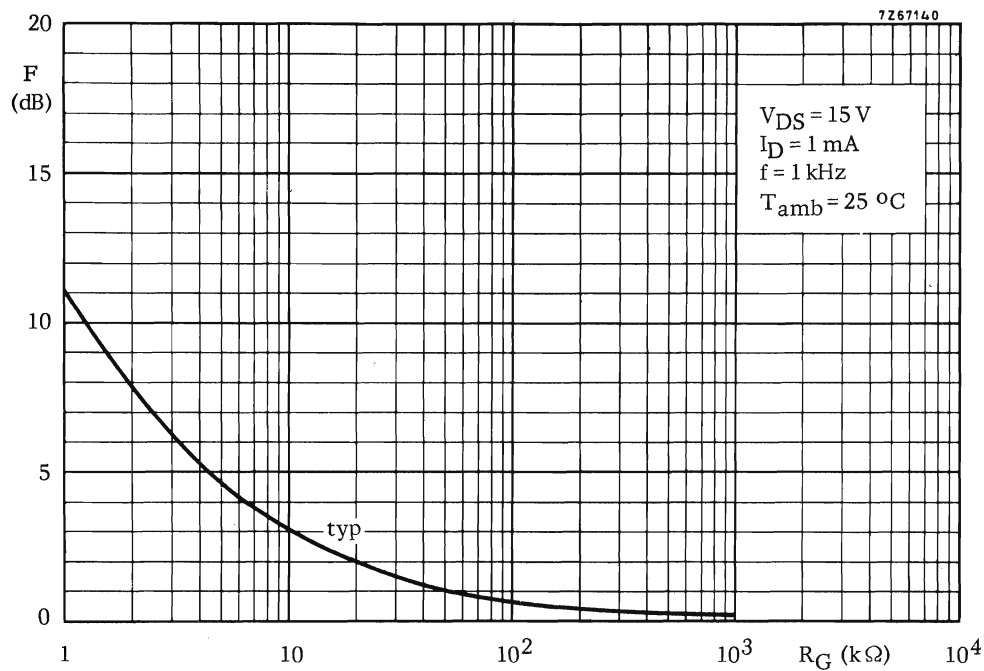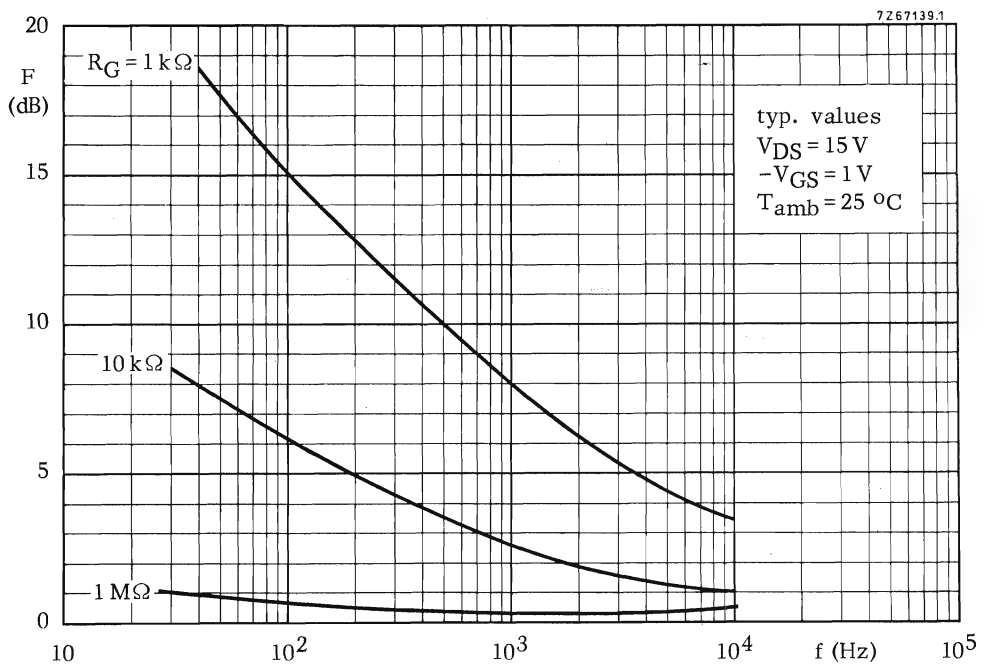
N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

General purpose symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for applications in l.f. and d.c. amplifiers, and in h.f. amplifiers.
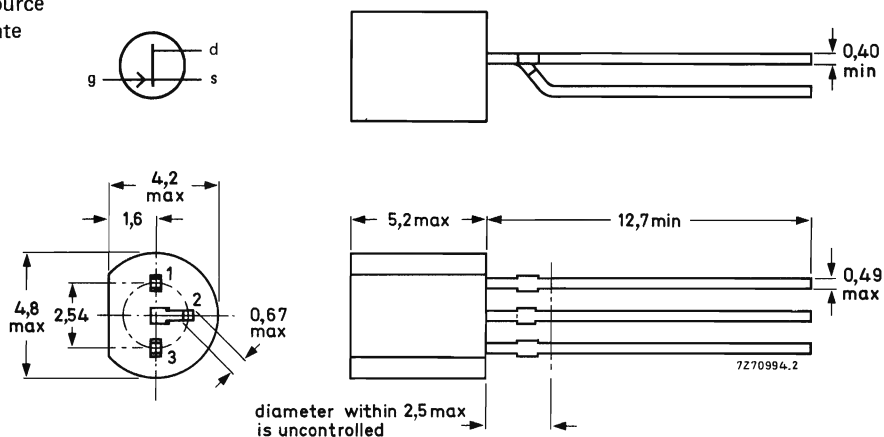
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Total power dissipation up to $T_{amb} = 75\ ^oC$	P_{tot}	max.	300	mW

		BF245A/0	A	B	C	
Drain current $V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}	$>$ 0,5 $<$ 2,1	2,0 6,5	6 15	12 25	mA mA

Gate-source cut-off voltage $I_D = 10$ nA; $V_{DS} = 15$ V	$-V_{(P)GS}$		0,25 to 8,0	V
Feedback capacitance at f = 1 MHz $V_{DS} = 20$ V; $-V_{GS} = 1$ V; $T_{amb} = 25\ ^oC$	C_{rs}	typ.	1,1	pF
Transfer admittance (common source) $V_{DS} = 15$ V; $V_{GS} = 0$; f = 1 kHz; $T_{amb} = 25\ ^oC$	$|Y_{fs}|$		3,0 to 6,5	mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:
1 = drain
2 = source
3 = gate

diameter within 2,5 max is uncontrolled

Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Drain current	I_D	max.	25	mA
Gate current	I_G	max.	10	mA
Power dissipation				
up to $T_{amb} = 75\ ^oC$	P_{tot}	max.	300	mW
up to $T_{amb} = 90\ ^oC$	P_{tot}	max.	300	mW 1)
Storage temperature	T_{stg}		-65 to $+150$	^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	0,25	K/mW
From junction to ambient	$R_{th\ j\text{-}a}$	=	0,20	K/mW 1)

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

		BF245A	B	C	
Gate cut-off current					
$-V_{GS} = 20$ V; $V_{DS} = 0$	$-I_{GSS}$	< 5	5	5	nA
$-V_{GS} = 20$ V; $V_{DS} = 0$; $T_j = 125\ ^oC$	$-I_{GSS}$	< 0,5	0,5	0,5	μA
Drain current 2)					
$V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS} 3)	> 2	6,0	12	mA
		< 6,5	15,0	25	mA
Gate-source breakdown voltage					
$-I_G = 1\ \mu A$; $V_{DS} = 0$	$-V_{(BR)GSS}$	> 30	30	30	V
Gate-source voltage					
$I_D = 200\ \mu A$; $V_{DS} = 15$ V	$-V_{GS}$ 3)	> 0,4	1,6	3,2	V
		< 2,2	3,8	7,5	V

1) Transistor mounted on printed circuit board, maximum lead length 3 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

2) Measured under pulse conditions: $t_p = 300\ \mu s$; $\delta \leqslant 0,02$.

3) BF245A/0: $I_{DSS} = 0,5$ to 2,1 mA; $-V_{GS} = 0,2$ to 1,0 V
   BF245A/1: $I_{DSS} = 1,9$ to 3,0 mA; $-V_{GS} = 0,4$ to 1,0 V
   BF245A/2: $I_{DSS} = 3,0$ to 4,5 mA; $-V_{GS} = 0,7$ to 1,4 V
   BF245A/3: $I_{DSS} = 4,5$ to 6,5 mA; $-V_{GS} = 1,1$ to 2,2 V.

Gate-source cut-off voltage

I_D = 10 nA; V_{DS} = 15 V $-V_{(P)GS}$ 0,25 to 8,0 V

y-parameters at T_{amb} = 25 °C (common source)

   V_{DS} = 15 V; V_{GS} = 0

f = 1 kHz	Transfer admittance	$|y_{fs}|$		3,0 to 6,5 mS
	Output admittance	$|y_{os}|$	typ.	25 μS
f = 200 MHz	Input conductance	g_{is}	typ.	250 μS
	Reverse transfer admittance	$|y_{rs}|$	typ.	1,4 mS
	Transfer admittance	$|y_{fs}|$	typ.	6 mS
	Output conductance	g_{os}	typ.	40 μS

   V_{DS} = 20 V; $-V_{GS}$ = 1 V

f = 1 MHz	Input capacitance	C_{is}	typ.	4,0 pF
	Feedback capacitance	C_{rs}	typ.	1,1 pF
	Output capacitance	C_{os}	typ.	1,6 pF

Cut-off frequency *

   V_{DS} = 15 V; V_{GS} = 0 f_{gfs} typ.   700 MHz

Noise figure at f = 100 MHz; R_G = 1 kΩ (common source)

   V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C
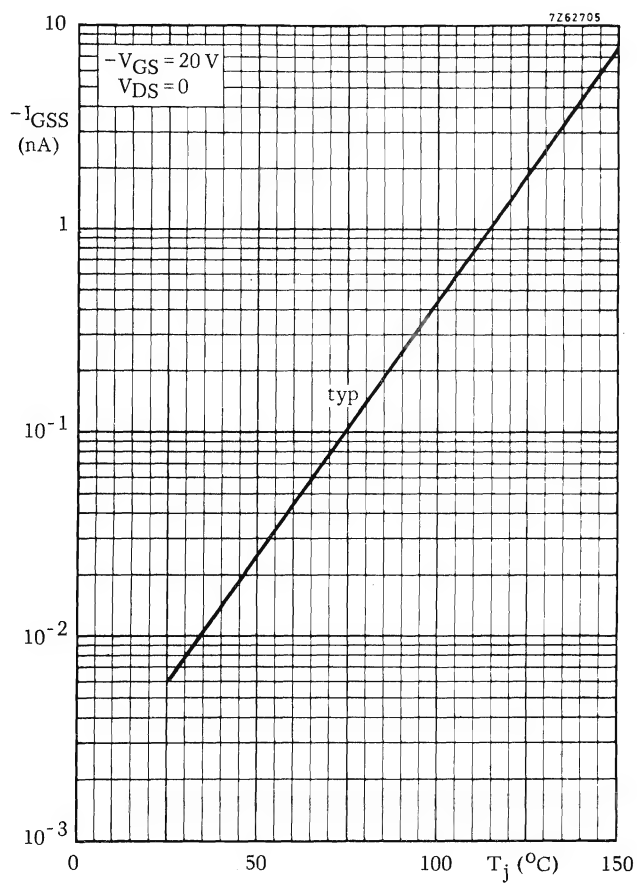input tuned to minimum noise   F   typ.   1,5 dB
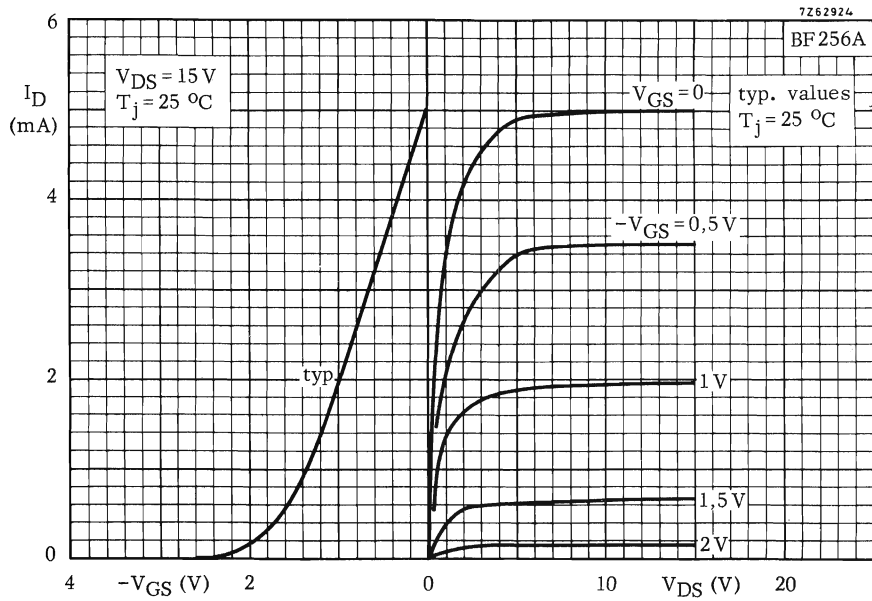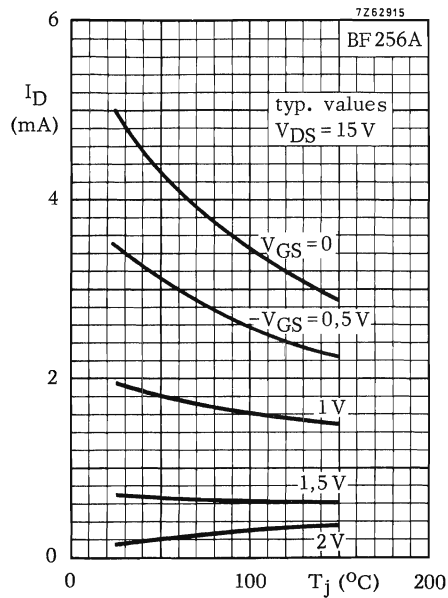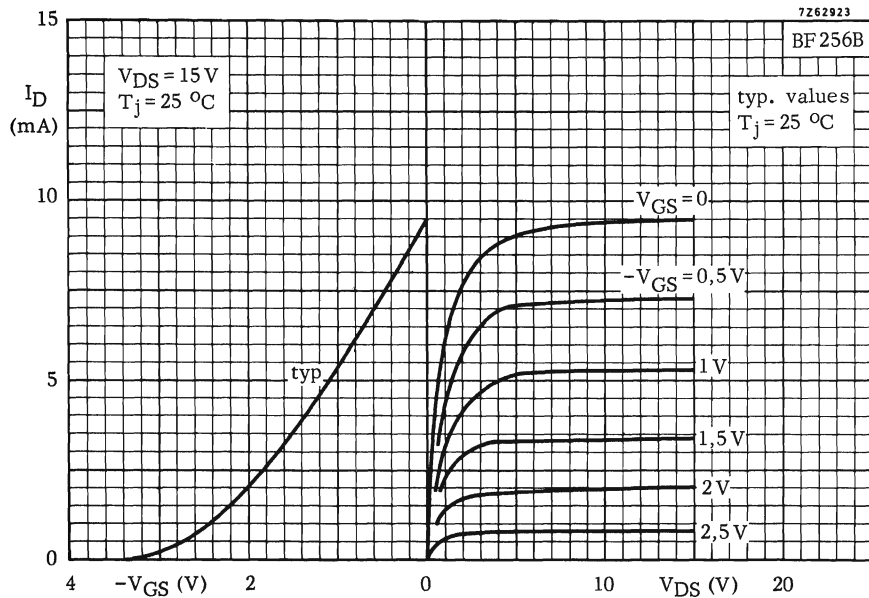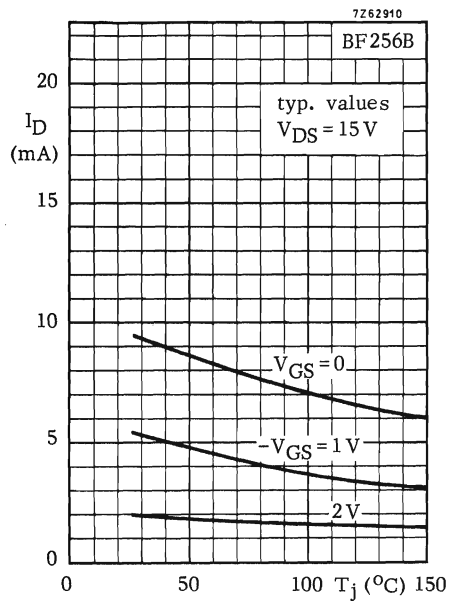
* The frequency at which g_{fs} is 0,7 of its value at 1 kHz.
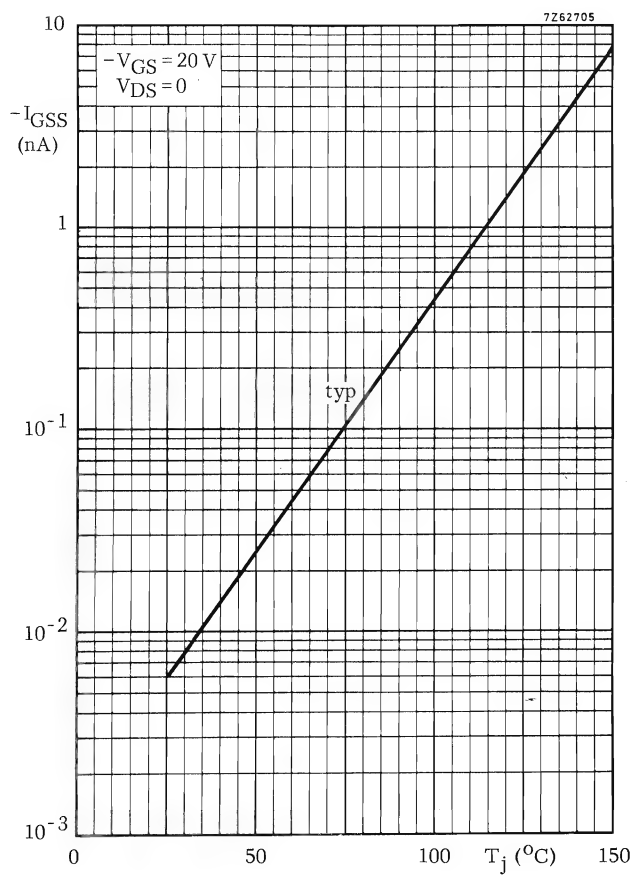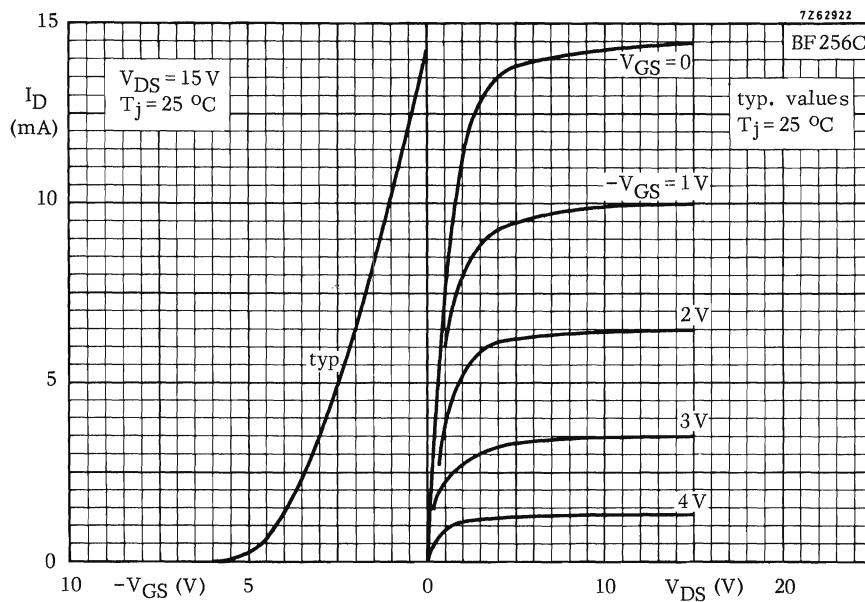
Fig. 2

Fig. 3

Fig. 4

Fig. 5

Fig. 6

Fig. 7

Fig. 8

7Z62698

typ. values
$V_{GS} = 0$
$V_{DS} = 15$ V
$T_{amb} = 25$ °C

g_{is}
(μA/V)

b_{is}
(mA/V)

g_{is}

b_{is}

f (MHz)

Fig. 9

7Z62700

typ. values
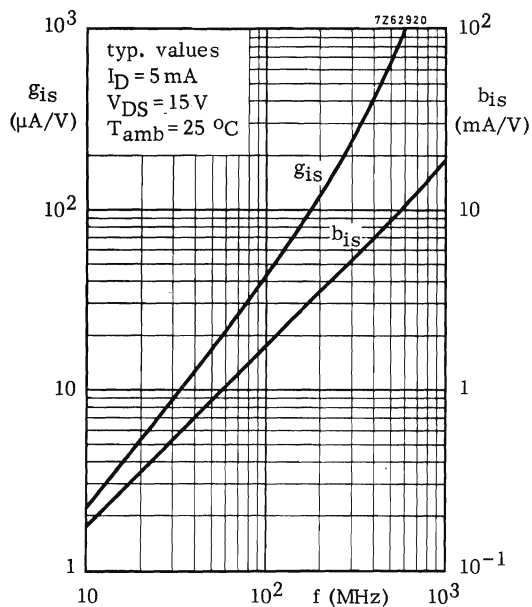$V_{GS} = 0$
$V_{DS} = 15$ V
$T_{amb} = 25$ °C

b_{rs}
(μA/V)

C_{rs}
(pF)

C_{rs}

b_{rs}

f (MHz)

Fig. 10

Fig. 11

Fig. 12

7Z62697

C_{is} (pF)

$V_{DS} = 20$ V
$T_{amb} = 25$ °C
$f = 1$ MHz

typ

$-V_{GS}$ (V)

Fig. 13

7Z62701

C_{rs} (pF)

$V_{DS} = 20$ V
$T_{amb} = 25$ °C
$f = 1$ MHz

typ

$-V_{GS}$ (V)

Fig. 14

7Z62723

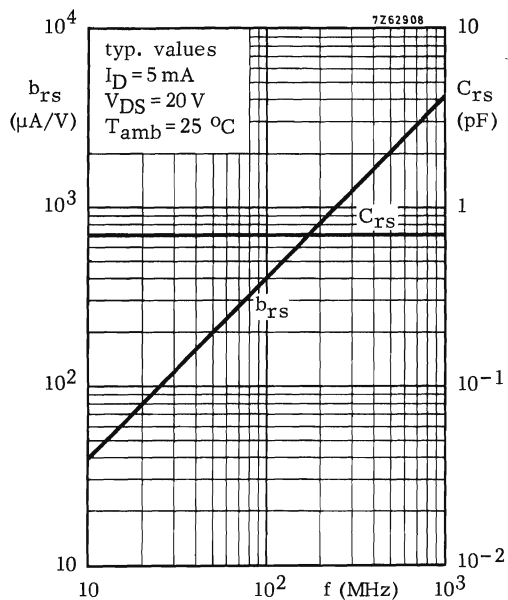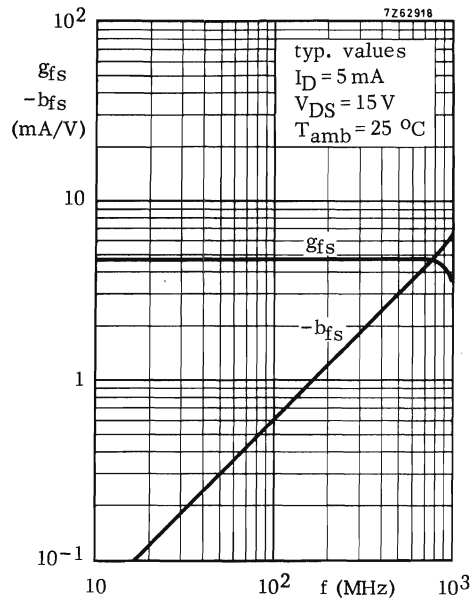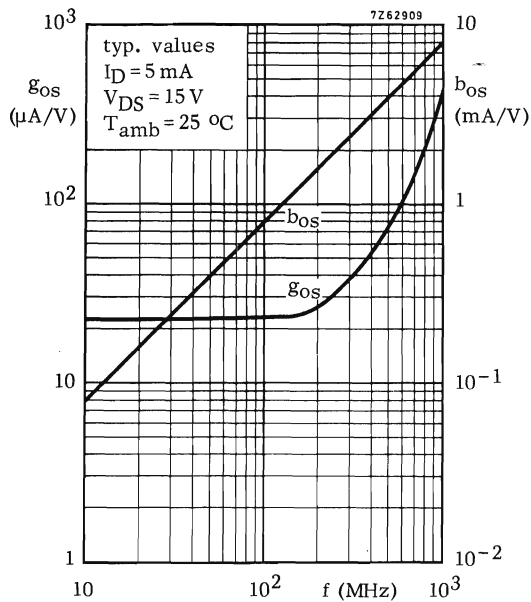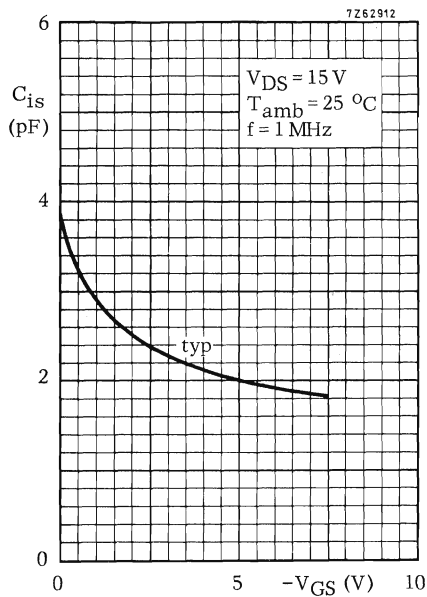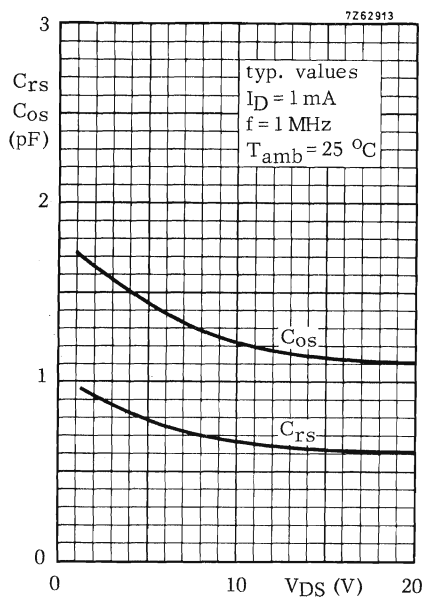$|y_{fs}|$ (mA/V)

typ. values
$V_{DS} = 15$ V
$f = 1$ kHz
$T_{amb} = 25$ °C

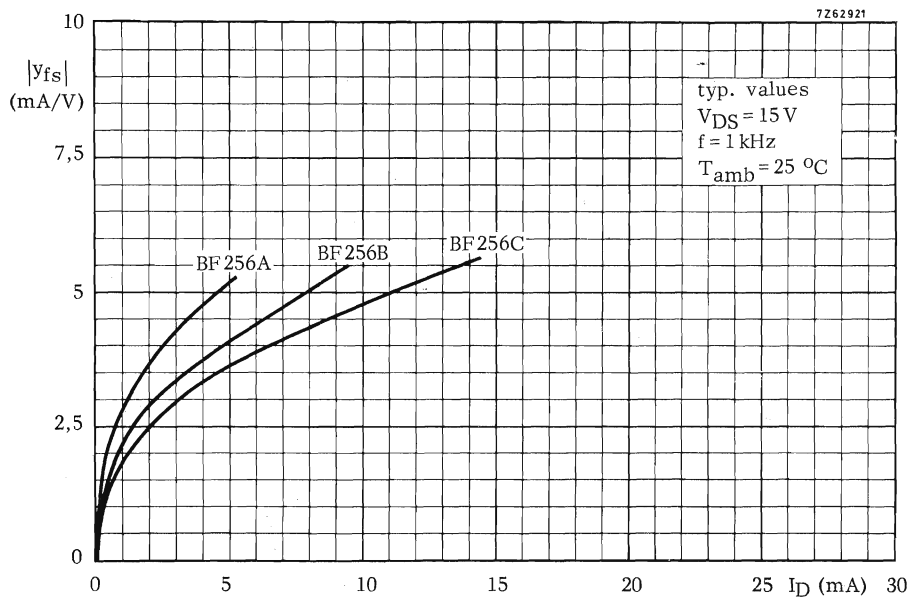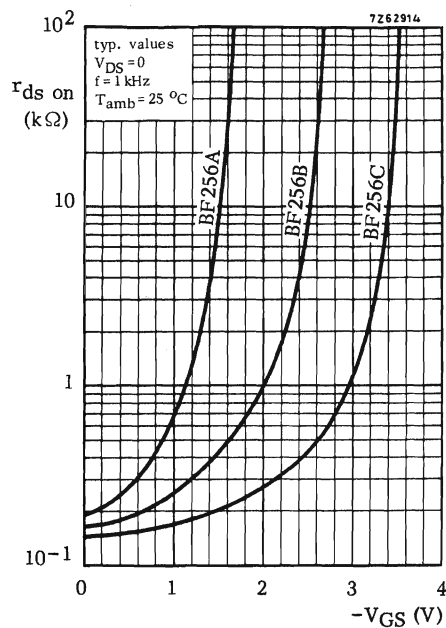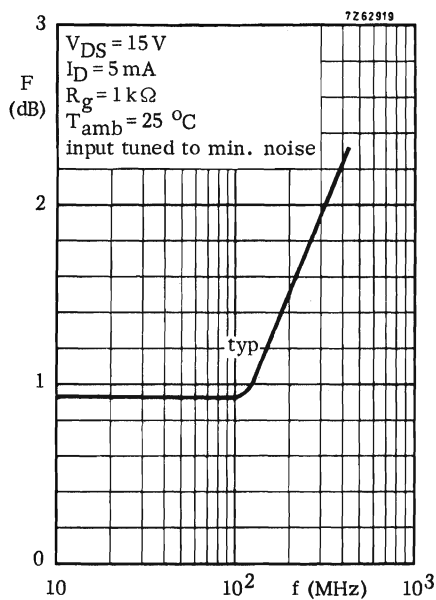BF245A

BF245B

BF245C

I_D (mA)
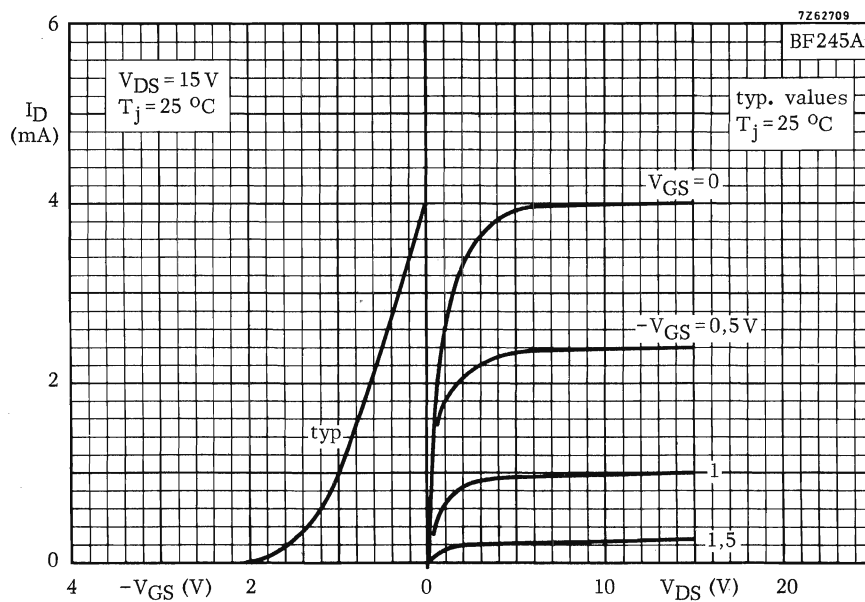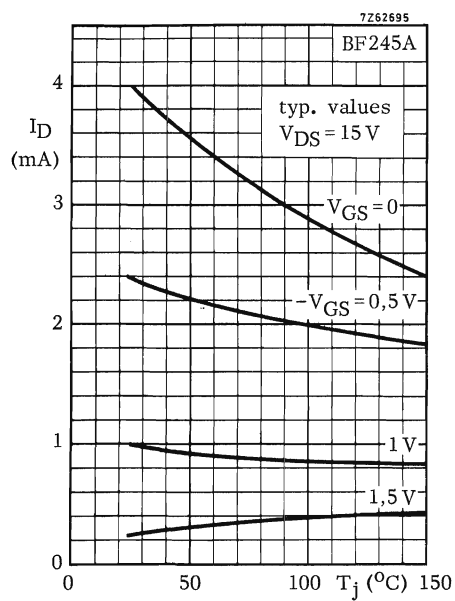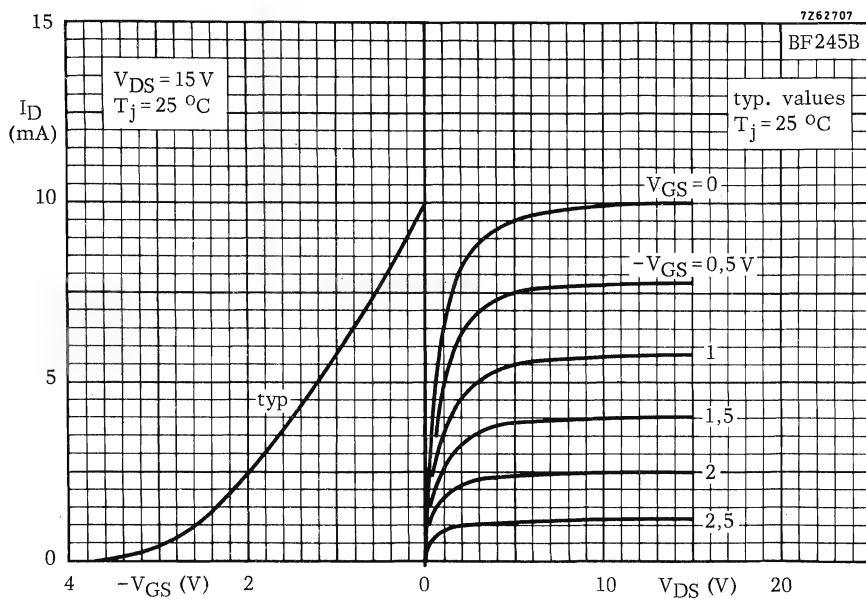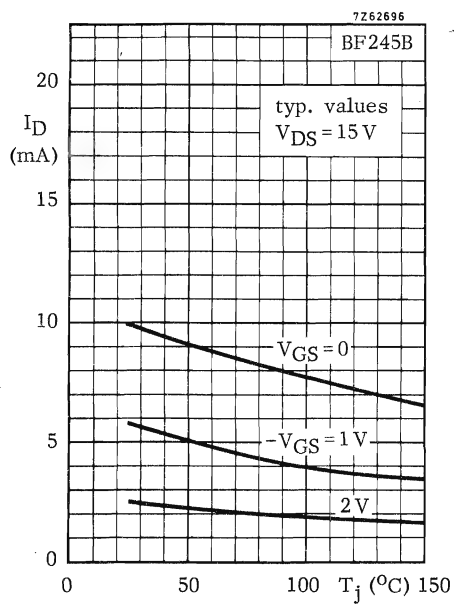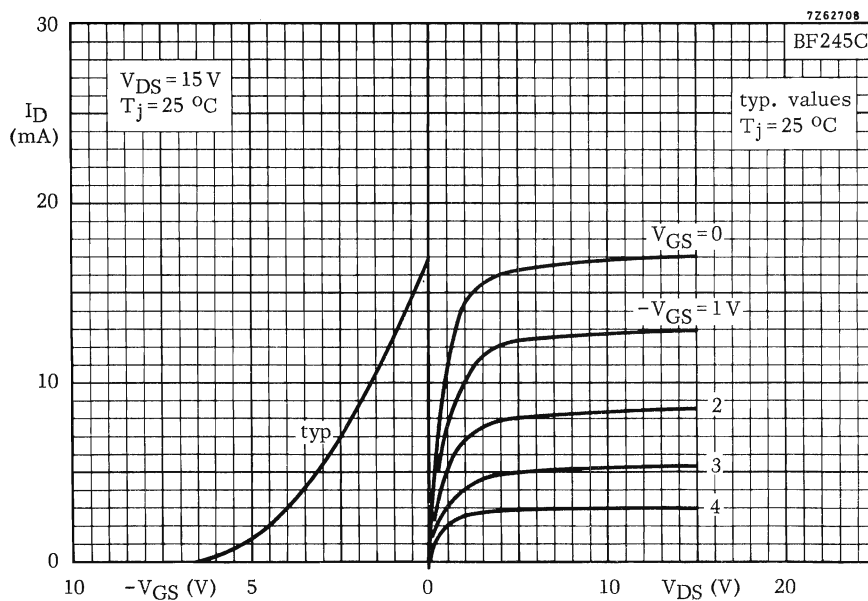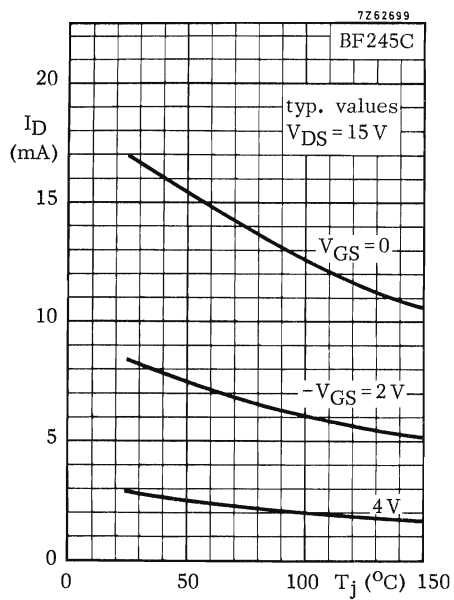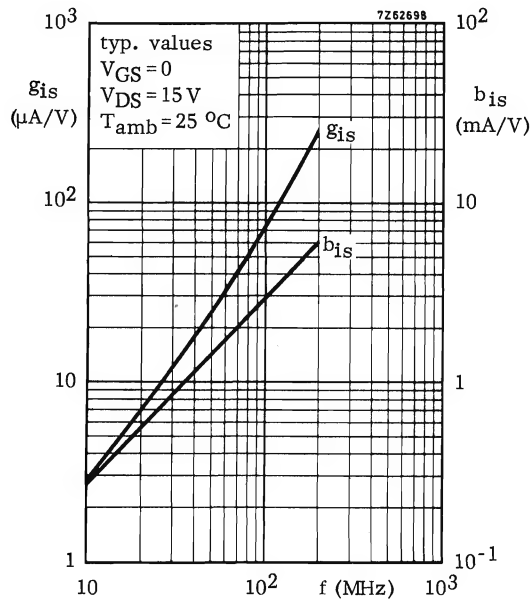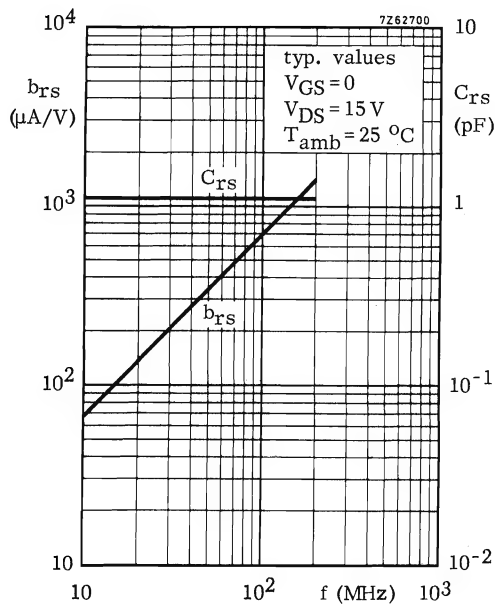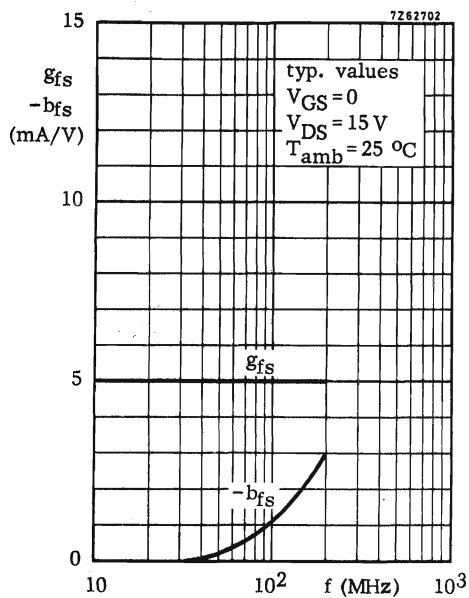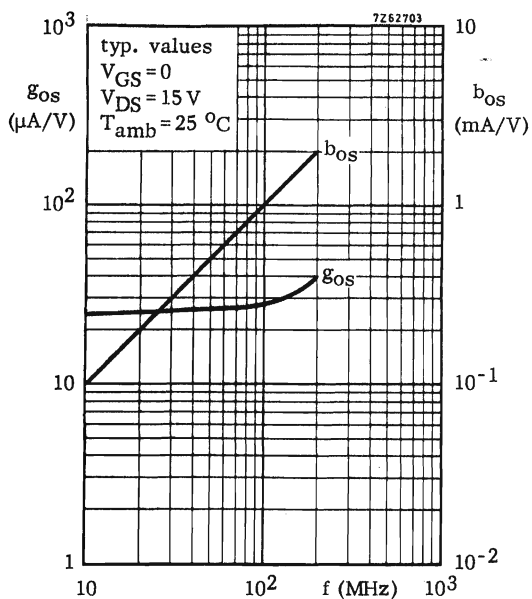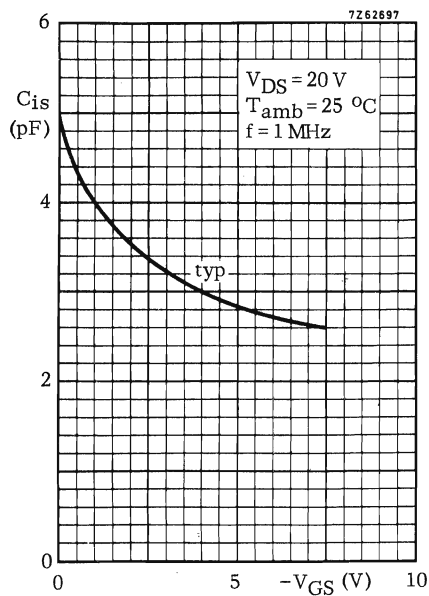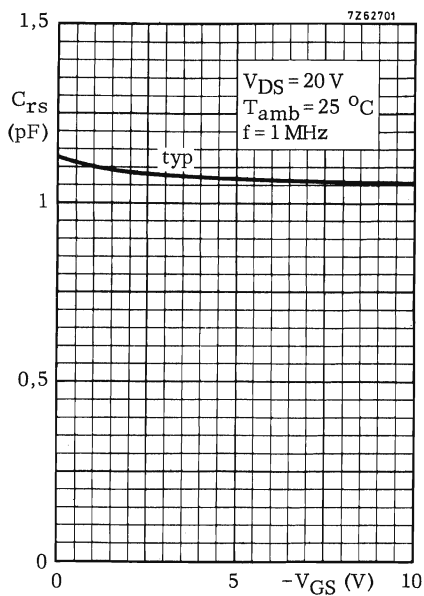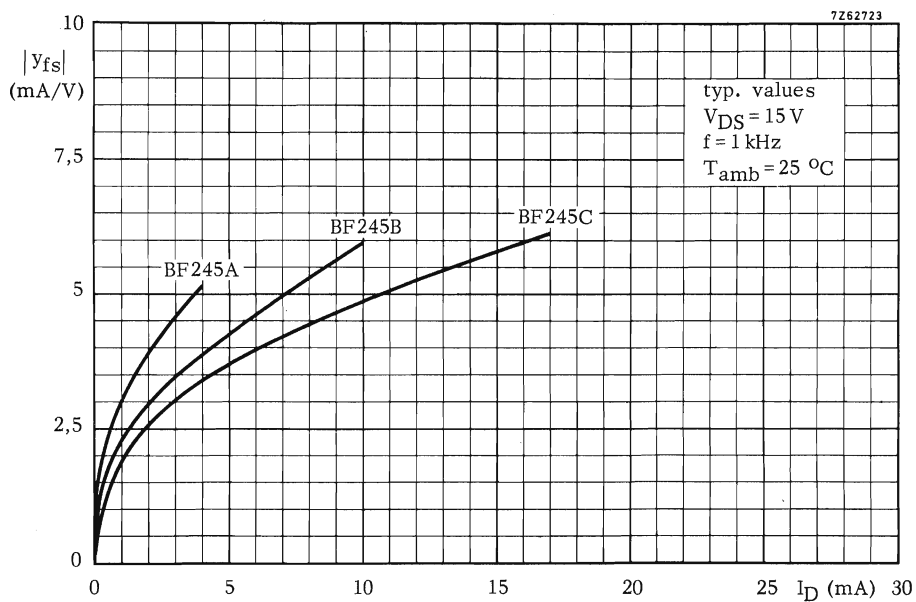
Fig. 15
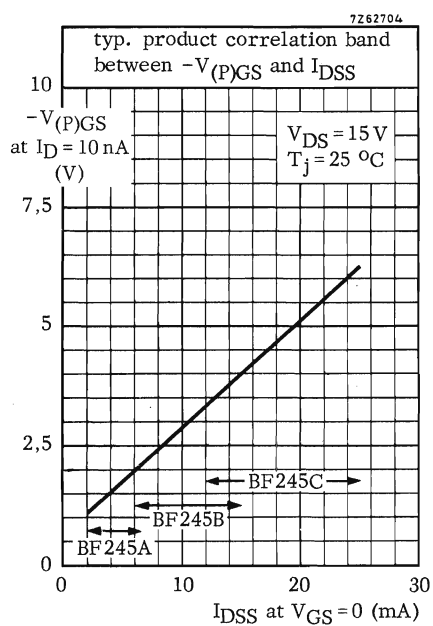
Fig. 16
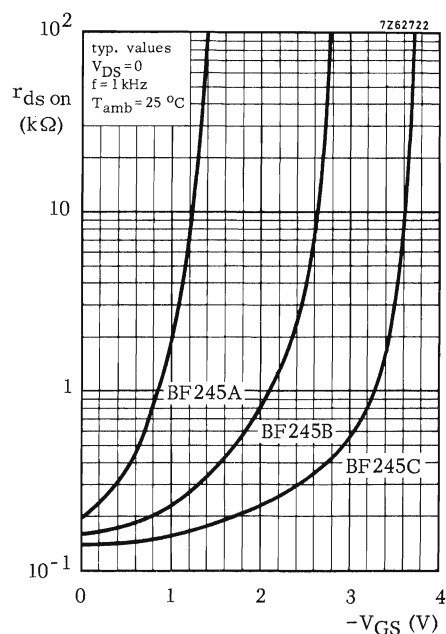
Fig. 17

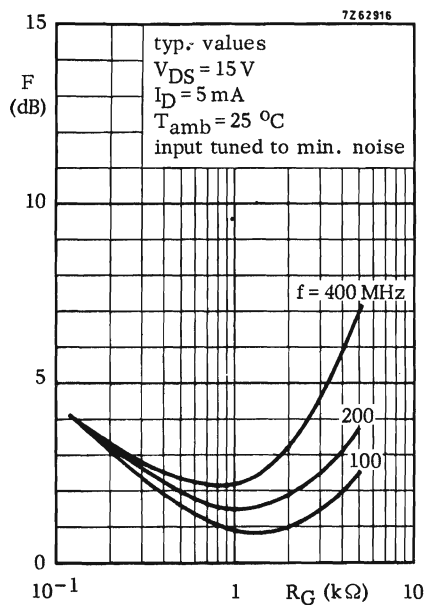Fig. 18

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical n-channel planar epitaxial junction field-effect transistors in plastic TO-92 variants, intended for v.h.f. and u.h.f. amplifiers, mixers, and general purpose switching.

QUICK REFERENCE DATA

			BF247A	B	C	
Drain-source voltage	$\pm V_{DS}$	max.			25	V
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.			250	mW
Drain current $V_{DS} = 15\ V; V_{GS} = 0$	I_{DSS}	$>$ $<$	30 80	60 140	110 250	mA mA
Gate-source cut-off voltage $I_D = 10\ nA; V_{DS} = 15\ V$	$-V_{(P)GS}$				0,6 to 14,5	V
Feedback capacitance at f = 1 MHz $I_D = 10\ mA; V_{DS} = 15\ V$	C_{rs}	typ.			3,5	pF
Transfer admittance (common source) $I_D = 10\ mA; V_{DS} = 15\ V; f = 1\ kHz$	$|y_{fs}|$	$>$			8	mS

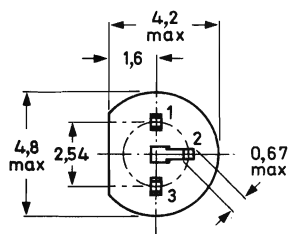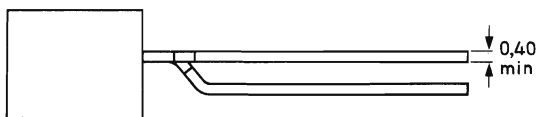## MECHANICAL DATA
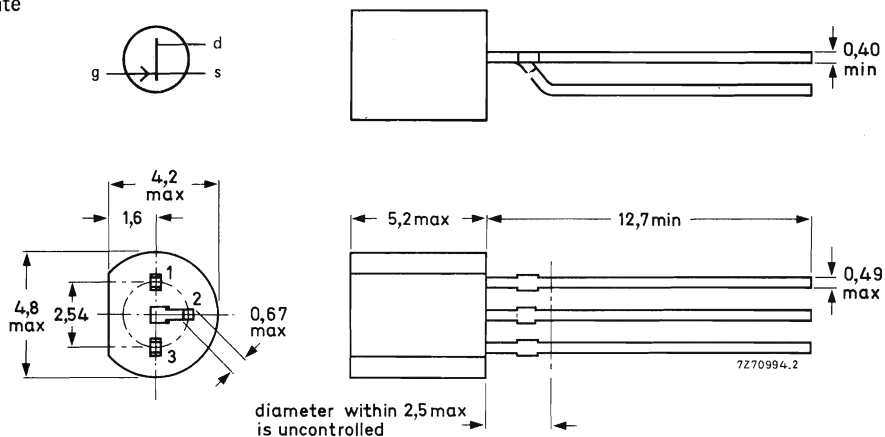
Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:
1 = drain
2 = source
3 = gate

diameter within 2,5 max is uncontrolled

7Z70994.2

Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Gate current	I_G	max.	10	mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	250	mW
Storage temperature	T_{stg}		-65 to $+150$	^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	500	K/W

CHARACTERISTICS

$T_{amb} = 25\ ^oC$

			BF247A	B	C	
Gate cut-off current $-V_{GS} = 15$ V; $V_{DS} = 0$	$-I_{GSS}$	$<$	5	5	5	nA
Drain current* $V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}	$>$	30	60	110	mA
		$<$	80	140	250	mA
Gate-source breakdown voltage $-I_G = 1\ \mu A$; $V_{DS} = 0$	$-V_{(BR)GSS}$	$>$	25	25	25	V
Gate-source voltage $I_D = 200\ \mu A$; $V_{DS} = 15$ V	$-V_{GS}$	$>$	1,5	3,0	5,5	V
		$<$	4,0	7,0	12,0	V
Gate-source cut-off voltage $I_D = 10$ nA; $V_{DS} = 15$ V	$-V_{(P)GS}$			0,6 to 14,5		V
Transfer admittance (common source) $I_D = 10$ mA; $V_{DS} = 15$ V; $f = 1$ kHz	$|y_{fs}|$	$>$		8		mS
		typ.		17		mS
Capacitances at $f = 1$ MHz $I_D = 10$ mA; $V_{DS} = 15$ V feed-back capacitance	C_{rs}	typ.		3,5		pF
input capacitance	C_{is}	typ.		11		pF
output capacitance	C_{cs}	typ.		5		pF
Cut-off frequency** $V_{DS} = 15$ V; $V_{GS} = 0$	f_{gfs}	typ.		450		MHz

* Measured under pulse conditions; $t_p = 300\ \mu s$; $\delta \leqslant 0,02$.
** The frequency at which g_{fs} is 0,7 of its value at 1 kHz.

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for v.h.f. and u.h.f. applications.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$			max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$			max.	30	V
Total power dissipation up to $T_{amb} = 75\,^oC$	P_{tot}			max.	300	mW
		BF256A	B	C		
Drain current		>3	6	11		mA
$V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}	<7	13	18		mA
Feedback capacitance at f = 1 MHz						
$V_{DS} = 20$ V; $-V_{GS} = 1$ V; $T_{amb} = 25\,^oC$	C_{rs}			typ.	0,7	pF
Transfer admittance (common source)						
$V_{DS} = 15$ V; $V_{GS} = 0$; f = 1 kHz; $T_{amb} = 25\,^oC$	$|Y_{fs}|$			$>$	4,5	mS
Power gain at f = 800 MHz						
$V_{DS} = 15$ V; $R_S = 47\ \Omega$	G_p			typ.	11	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning;
1 = drain
2 = source
3 = gate

diameter within 2,5 max
is uncontrolled

7Z70994.2

Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Gate current	I_G	max.	10	mA
Total power dissipation				
up to $T_{amb} = 75\ ^oC$	P_{tot}	max.	300	mW
up to $T_{amb} = 90\ ^oC$	P_{tot}	max.	300	mW 1)
Storage temperature	T_{stg}	-65 to $+150$		^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250	K/W
From junction to ambient	$R_{th\ j\text{-}a}$	=	200	K/W 1)

CHARACTERISTICS

$T_{amb} = 25\ ^oC$ unless otherwise specified

Gate cut-off current
$-V_{GS} = 20$ V; $V_{DS} = 0$ $-I_{GSS}$ $<$ 5 nA

Drain current 2)

		BF256A	B	C	
$V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS} 3) $>$	3	6	11	mA
	$<$	7	13	18	mA

Gate-source breakdown voltage
$-I_G = 1\ \mu A$; $V_{DS} = 0$ $-V_{(BR)GSS}$ $>$ 30 V

Gate-source voltage
$I_D = 200\ \mu A$; $V_{DS} = 15$ V $-V_{GS}$ 3)   0,5 to 7,5 V

1) Transistor mounted on printed circuit board, maximum lead length 3 mm, mounting pad for drain
   lead minimum 10 mm x 10 mm.

2) Measured under pulse conditions: $t_p = 300\ \mu s$; $\delta \leqslant 0{,}02$.

3) BF256B/1: $I_{DSS} = 6$ to 8 mA; $-V_{GS} = 1{,}4$ to 2,6 V.

y-parameters (common source)

Transistor admittance at f = 1 kHz			
V_{DS} = 15 V; V_{GS} = 0	$|y_{fs}|$	>	4,5 mS 1)
		typ.	5 mS 1)
Output capacitance at f = 1 MHz			
V_{DS} = 20 V; V_{GS} = 0	C_{os}	typ.	1,2 pF
Feedback capacitance at f = 1 MHz			
V_{DS} = 20 V; $-V_{GS}$ = 1 V	C_{rs}	typ.	0,7 pF
Cut-off frequency			
V_{DS} = 15 V; V_{GS} = 0	f_{gfs}	typ.	1 GHz 2)
Noise figure at f = 800 MHz			
V_{DS} = 10 V; R_S = 47 Ω	F	typ.	7,5 dB
Power gain at f = 800 MHz			
V_{DS} = 15 V; R_S = 47 Ω	G_p	typ.	11 dB

1) Measured under pulse conditions: t_p = 300 μs; $\delta \leqslant 0,02$.

2) The frequency at which g_{fs} is 0,7 of its value at 1 kHz.

Fig. 2

Fig. 3

Fig. 4

7Z62923

BF 256B

$V_{DS} = 15 V$
$T_j = 25$ °C

typ. values
$T_j = 25$ °C

I_D (mA)

$V_{GS} = 0$

$-V_{GS} = 0,5 V$

1 V

1,5 V

2 V

2,5 V

typ

$-V_{GS} (V)$ $V_{DS} (V)$

Fig. 5

7Z62910

BF 256B

I_D (mA)

typ. values
$V_{DS} = 15 V$

$V_{GS} = 0$

$-V_{GS} = 1 V$

2 V

T_j (°C)

Fig. 6

7Z62922

BF256C

$V_{DS} = 15\,V$
$T_j = 25\,^{\circ}C$

I_D
(mA)

$V_{GS} = 0$

typ. values
$T_j = 25\,^{\circ}C$

$-V_{GS} = 1\,V$

typ.

2 V

3 V

4 V

$-V_{GS}$ (V) V_{DS} (V)

Fig. 7

7Z62911

BF256C

I_D
(mA)

typ. values
$V_{DS} = 15\,V$

$V_{GS} = 0$

$-V_{GS} = 2\,V$

4 V

T_j ($^{\circ}C$)

Fig. 8

Fig. 9

Fig. 10

7Z62918

g_{fs}
$-b_{fs}$
(mA/V)

typ. values
$I_D = 5\,mA$
$V_{DS} = 15\,V$
$T_{amb} = 25\ ^{o}C$

g_{fs}

$-b_{fs}$

f (MHz)

Fig. 11

7Z62909

g_{os}
(μA/V)

b_{os}
(mA/V)

typ. values
$I_D = 5\,mA$
$V_{DS} = 15\,V$
$T_{amb} = 25\ ^{o}C$

$-b_{os}$

g_{os}

f (MHz)

Fig. 12

7Z62912

C_{is}
(pF)

$V_{DS} = 15 \text{ V}$
$T_{amb} = 25 \text{ }^{\circ}C$
$f = 1 \text{ MHz}$

typ

$-V_{GS}$ (V)

Fig. 13

7Z62913

C_{rs}
C_{os}
(pF)

typ. values
$I_D = 1 \text{ mA}$
$f = 1 \text{ MHz}$
$T_{amb} = 25 \text{ }^{\circ}C$

C_{os}

C_{rs}

V_{DS} (V)

Fig. 14

7Z62921

$|y_{fs}|$
(mA/V)

typ. values
$V_{DS} = 15 \text{ V}$
$f = 1 \text{ kHz}$
$T_{amb} = 25 \text{ }^{\circ}C$

BF 256A   BF 256B   BF 256C

I_D (mA)

Fig. 15

7Z62914

typ. values
$V_{DS} = 0$
$f = 1\,kHz$
$T_{amb} = 25\,^oC$

$r_{ds\ on}$ (kΩ)

BF256A

BF256B

BF256C

$-V_{GS}$ (V)

Fig. 16

7Z62919

$V_{DS} = 15\,V$
$I_D = 5\,mA$
$R_g = 1\,k\Omega$
$T_{amb} = 25\,^oC$
input tuned to min. noise

F (dB)

typ.

f (MHz)

Fig. 17

7Z62916

typ. values
$V_{DS} = 15\,V$
$I_D = 5\,mA$
$T_{amb} = 25\,^oC$
input tuned to min. noise

F (dB)

$f = 400\,MHz$

200

100

R_G (kΩ)

Fig. 18

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Asymmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for applications up to the v.h.f. range.

These FETs can be supplied in four I_{DSS} groups. Special features are the low feedback capacitance and the low noise figure. Thanks to these special features the BF410 is very suitable for applications such as the r.f. stages in f.m. portables (type A), car radios (type B) and mains radios (type C) or the mixer stage (type D).

QUICK REFERENCE DATA

			BF410A	B	C	D	
Drain-source voltage	V_{DS}	max.		20			V
Drain current (d.c. or average)	I_D	max.		30			mA
Total power dissipation up to $T_{amb} = 75\ ^oC$	P_{tot}	max.		300			mW
Drain current $V_{DS} = 10$ V; $V_{GS} = 0$	I_{DSS}	> <	0,7 3,0	2,5 7,0	6 12	10 18	mA mA
Transfer admittance (common source) $V_{DS} = 10$ V; $V_{GS} = 0$; f = 1 kHz	$\lvert y_{fs} \rvert$	>	2,5	4	6	7	mS
Feedback capacitance $V_{DS} = 10$ V; $V_{GS} = 0$	C_{rs}	typ.	0,3	0,3	—	—	pF
$V_{DS} = 10$ V; $I_D = 5$ mA	C_{rs}	typ.	—	—	0,3	0,3	pF
Noise figure at optimum source admittance $G_S = 1$ mS; $-B_S = 3$ mS; f = 100 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	F	typ.	1,5	1,5	—	—	dB
$V_{DS} = 10$ V; $I_D = 5$ mA	F	typ.	—	—	1,5	1,5	dB

MECHANICAL DATA
Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:
1 = drain
2 = source
3 = gate

4,2 max
1,6
4,8 max
2,54
0,67 max
5,2 max
12,7 min
0,40 min
0,49 max
diameter within 2,5 max is uncontrolled
7Z70994.2

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain-gate voltage (open source)	V_{DGO}	max.	20	V
Drain current (d.c. or average)	I_D	max.	30	mA
Gate current	$\pm I_G$	max.	10	mA
Total power dissipation up to $T_{amb} = 75\ ^oC$	P_{tot}	max.	300	mW
Storage temperature	T_{stg}		-65 to $+150$	^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250	K/W

STATIC CHARACTERISTICS

$T_{amb} = 25\ ^oC$

			BF410A	B	C	D	
Gate cut-off current $-V_{GS} = 0,2$ V; $V_{DS} = 0$	$-I_{GSS}$	$<$	10	10	10	10	nA
Gate-drain breakdown voltage $I_S = 0$; $-I_D = 10\ \mu A$	$-V_{(BR)GDO}$	$>$	20	20	20	20	V
Drain current $V_{DS} = 10$ V; $V_{GS} = 0$	I_{DSS}	$>$ $<$	0,7 3,0	2,5 7,0	6 12	10 18	mA mA
Gate-source cut-off voltage $I_D = 10\ \mu A$; $V_{DS} = 10$ V	$-V_{(P)GS}$	typ.	0,8	1,5	2,2	3	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $V_{DS} = 10$ V; $V_{GS} = 0$; $T_{amb} = 25$ °C for **BF410A** and **B**

$V_{DS} = 10$ V; $I_D = 5$ mA; $T_{amb} = 25$ °C for **BF410C** and **D**

y-parameters (common source)			BF410A	B	C	D	
Input capacitance at f = 1 MHz	C_{is}	<	5	5	5	5	pF
Input conductance at f = 100 MHz	g_{is}	typ.	100	90	60	50	μS
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	0,3	0,3	0,3	0,3	pF
		<	0,4	0,4	0,4	0,4	pF
Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	>	2,5	4,0	4,0	3,5	mS
$V_{GS} = 0$ instead of $I_D = 5$ mA	$\lvert y_{fs} \rvert$	>	–	–	6,0	7,0	mS
Transfer admittance at f = 100 MHz	$\lvert y_{fs} \rvert$	typ.	3,5	5,5	5,0	5,0	mS
Output capacitance at f = 1 MHz	C_{os}	<	3	3	3	3	pF
Output conductance at f = 1 MHz	g_{os}	<	60	80	100	120	μS
Output conductance at f = 100 MHz	g_{os}	typ.	35	55	70	90	μS
Noise figure at optimum source admittance							
$G_S = 1$ mS; $-B_S = 3$ mS; f = 100 MHz	F	typ.	1,5	1,5	1,5	1,5	dB

7Z74941

Fig. 2 V_{GS} = 0 for **BF410A** and **BF410B**;
I_D = 5 mA for **BF410C** and **BF410D**;
f = 1 MHz; T_{amb} = 25 °C.

7Z74942
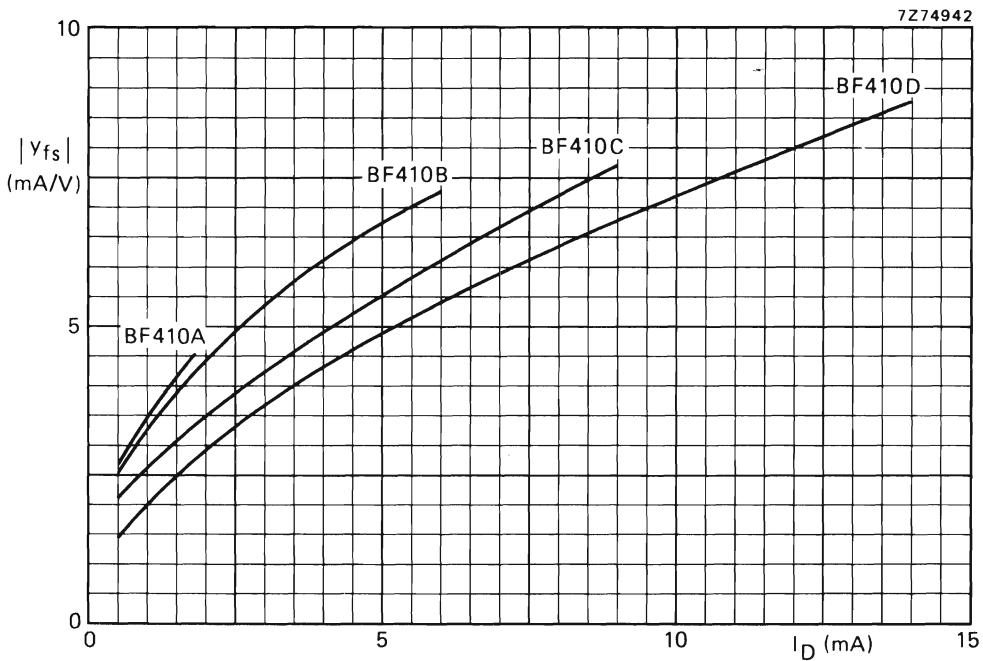
Fig. 3 V_{DS} = 10 V; f = 1 kHz; T_{amb} = 25 °C; typical values.

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Asymmetrical N-channel planar epitaxial junction field-effect transistors in the miniature plastic
envelope intended for applications up to the v.h.f. range in hybrid thick and thin-film circuits. Special
features are the low feedback capacitance and the low noise figure. These features make the product
very suitable for applications such as the r.f. stages in f.m. portables (BF510), car radios (BF511) and
mains radios (BF512) or the mixer stage (BF513).

QUICK REFERENCE DATA

			BF510	511	512	513	
Drain-source voltage	V_{DS}	max.		20			V
Drain current (d.c. or average)	I_D	max.		30			mA
Total power dissipation up to $T_{amb} = 65\ ^oC$	P_{tot}	max.		250			mW
Drain current $V_{DS} = 10$ V; $V_{GS} = 0$	I_{DSS}	> <	0,7 3,0	2,5 7,0	6 12	10 18	mA mA
Transfer admittance (common source) $V_{DS} = 10$ V; $V_{GS} = 0$; f = 1 kHz	$|y_{fs}|$	>	2,5	4	6	7	mS
Feedback capacitance $V_{DS} = 10$ V; $V_{GS} = 0$	C_{rs}	typ.	0,3	0,3	–	–	pF
$V_{DS} = 10$ V; $I_D = 5$ mA	C_{rs}	typ.	–	–	0,3	0,3	pF
Noise figure at optimum source admittance $G_S = 1$ mS; $-B_S = 3$ mS; f = 100 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	F	typ.	1,5	1,5	–	–	dB
$V_{DS} = 10$ V; $I_D = 5$ mA	F	typ.	–	–	1,5	1,5	dB

MECHANICAL DATA
SOT-23.

See also *Soldering recommendations.*

MECHANICAL DATA

Fig. 1 SOT-23
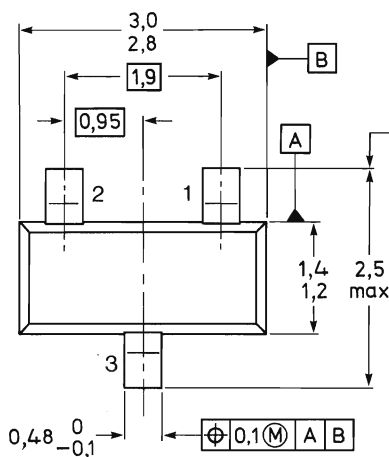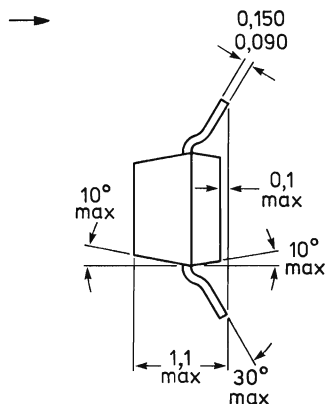
Dimensions in mm

TOP VIEW

Marking code

BF510 = S6
BF511 = S7
BF512 = S8
BF513 = S9

7Z96885

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage see Fig. 4	V_{DS}	max.	20	V
Drain-gate voltage (open source) see Fig. 4	V_{DGO}	max.	20	V
Drain current (d.c. or average)	I_D	max.	30	mA
Gate current	$\pm I_G$	max.	10	mA
Total power dissipation up to T_{amb} = 60 °C**	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}	−65 to + 175		°C
Junction temperature	T_j	max.	175	°C

THERMAL CHARACTERISTICS*

$$T_j = Px \, (R_{th\,j\text{-}t} + R_{th\,t\text{-}s} + R_{th\,s\text{-}a}) + T_{amb}$$

Thermal resistance

From junction to tab	$R_{th\,j\text{-}t}$	=	60	K/W
From tab to soldering points	$R_{th\,t\text{-}s}$	=	280	K/W
From soldering points to ambient**	$R_{th\,s\text{-}a}$	=	90	K/W

*   See *Thermal characteristics.*
** Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

STATIC CHARACTERISTICS

T_{amb} = 25 °C

			BF510	511	512	513	
Gate cut-off current $-V_{GS}$ = 0,2 V; V_{DS} = 0	$-I_{GSS}$	<	10	10	10	10	nA
Gate-drain breakdown voltage I_S = 0; $-I_D$ = 10 μA	$-V_{(BR)GDO}$	>	20	20	20	20	V
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	> <	0,7 3,0	2,5 7,0	6 12	10 18	mA mA
Gate-source cut-off voltage I_D = 10 μA; V_{DS} = 10 V	$-V_{(P)GS}$	typ.	0,8	1,5	2,2	3	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C for BF510 and BF511

V_{DS} = 10 V; I_D = 5 mA; T_{amb} = 25 °C for BF512 and BF513

y-parameters (common source)			BF510	511	512	513	
Input capacitance at f = 1 MHz	C_{is}	<	5	5	5	5	pF
Input conductance at f = 100 MHz	g_{is}	typ.	100	90	60	50	μS
Feedback capacitance at f = 1 MHz	C_{rs}	typ. <	0,3 0,4	0,3 0,4	0,3 0,4	0,3 0,4	pF pF
Transfer admittance at f = 1 kHz	$|y_{fs}|$	>	2,5	4,0	4,0	3,5	mS
V_{GS} = 0 instead of I_D = 5 mA	$|y_{fs}|$	>	–	–	6,0	7,0	mS
Transfer admittance at f = 100 MHz	$|y_{fs}|$	typ.	3,5	5,5	5,0	5,0	mS
Output capacitance at f = 1 MHz	C_{os}	<	3	3	3	3	pF
Output conductance at f = 1 MHz	g_{os}	<	60	80	100	120	μS
Output conductance at f = 100 MHz	g_{os}	typ.	35	55	70	90	μS
Noise figure at optimum source admittance G_S = 1 mS; $-B_S$ = 3 mS; f = 100 MHz	F	typ.	1,5	1,5	1,5	1,5	dB

7Z74941

Fig. 2 $V_{GS} = 0$ for BF510 and BF511;
$I_D = 5$ mA for BF512 and BF513;
$f = 1$ MHz; $T_{amb} = 25$ °C.
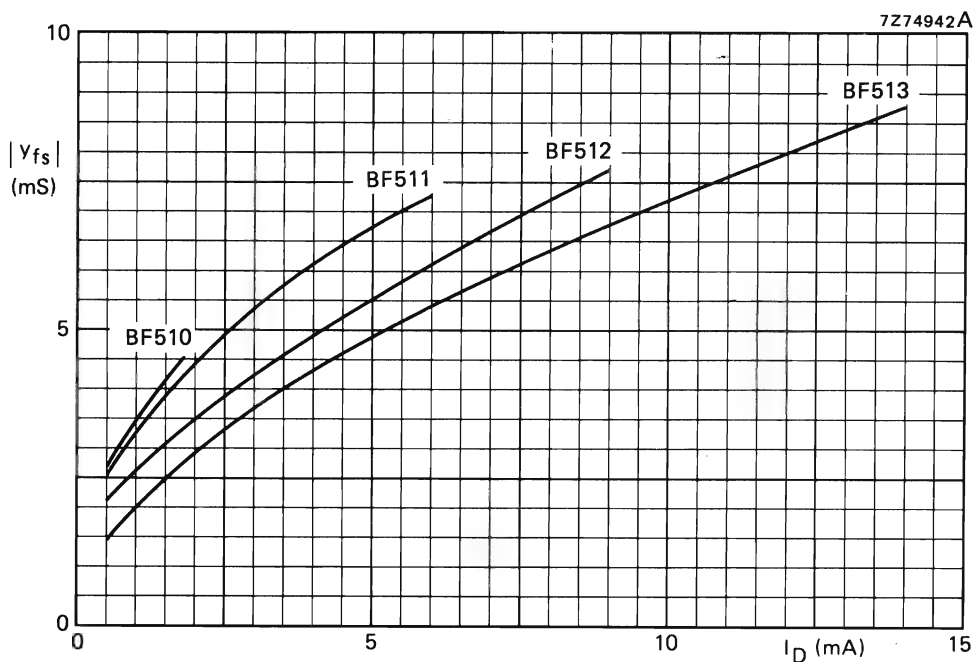
7Z74942A

Fig. 3 $V_{DS} = 10$ V; $f = 1$ kHz; $T_{amb} = 25$ °C; typical values.

7Z82719.1

Fig. 4 Voltage derating curve.

7Z82718
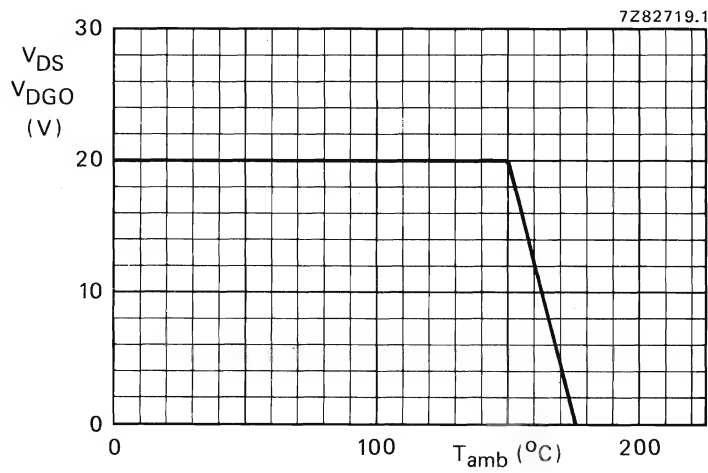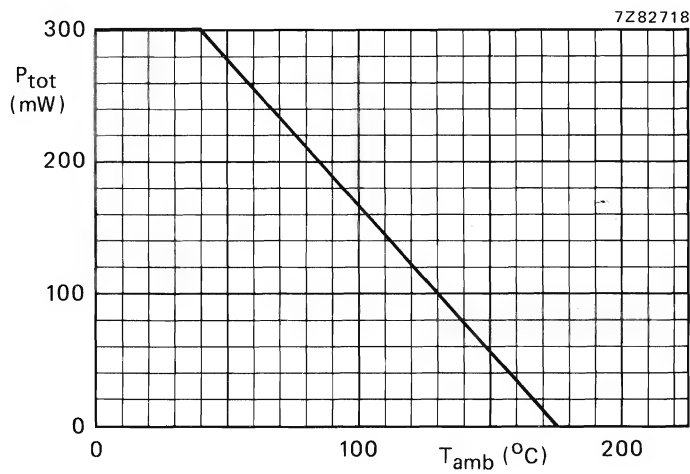
Fig. 5 Power derating curve.

DUAL N-CHANNEL FETS

Dual symmetrical n-channel silicon planar epitaxial junction field-effect transistors in a TO-71 metal envelope, with electrically insulated gates and a common substrate connected to the envelope; intended for high performance low level differential amplifiers.

QUICK REFERENCE DATA

Characteristics measured at T_{amb} = 25 °C; I_D = 200 μA; V_{DG} = 15 V

			BFQ10	11	12	13	14	15	16	
Difference in gate current	$\|\Delta I_G\|$	<	10	10	10	10	10	10	10	pA
Gate-source voltage difference	$\|\Delta V_{GS}\|$	<	5	10	10	10	15	20	50	mV
Thermal drift of gate-source voltage difference	$\left\|\dfrac{d\Delta V_{GS}}{dT}\right\|$	<	5	5	10	20	20	40	50	μV/K
Transfer conductance ratio	$\dfrac{g_{1fs}}{g_{2fs}}$	> <	0,98 1,02	0,98 1,02	0,98 1,02	0,98 1,02	0,98 1,02	0,95 1,05	0,95 1,05	
Difference in transfer impedance	$\left\|\Delta \dfrac{1}{g_{fs}}\right\|$	<	6	6	12	12	12	20	30	Ω
Difference in penetration factor	$\left\|\Delta \dfrac{g_{os}}{g_{fs}}\right\|$	<	10	30	40	50	60	70	100	μV/V
Common mode rejection ratio	CMRR	>	100	90	90	90	90	90	80	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-71.

All leads insulated from the case.
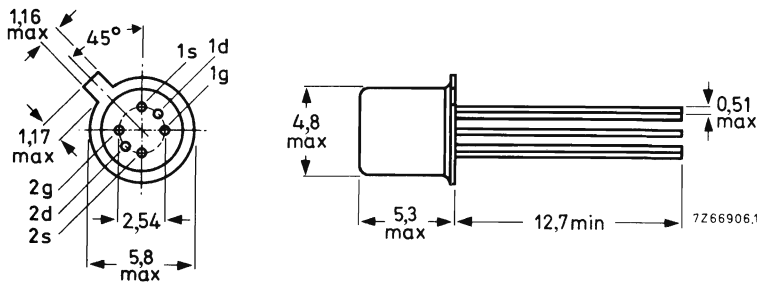
RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Voltage between gate 1 and gate 2	$\pm V_{1G-2G}$	max.	40	V
Drain current	I_D	max.	30	mA
Gate current	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 75 ^oC	P_{tot}	max.	250	mW
Storage temperature	T_{stg}	−65 to +200		^oC
Junction temperature	T_j	max.	200	^oC

THERMAL RESISTANCE

From junction to ambient in free air $\quad\quad R_{th\ j-a}$ = 500 K/W

CHARACTERISTICS (total device)

$T_{amb} = 25\ ^oC$ unless otherwise specified

Measured at: $I_D = 200\ \mu A$; $V_{DG} = 15\ V$ except for drain current ratio.

		BFQ10	11	12	13	14	15	16	
Drain current ratio [1] $V_{DG} = 15\ V$; $V_{GS} = 0$	$\dfrac{I_{1D-1SS}}{I_{2D-2SS}}$	> 0,97 < 1,03	0,95 1,05	0,95 1,05	0,95 1,05	0,92 1,08	0,90 1,10	0,80 1,20	
Difference in gate current	$\left\|\Delta I_G\right\|$	< 10	10	10	10	10	10	10	pA
Gate-source voltage difference	$\left\|\Delta V_{GS}\right\|$	< 5	10	10	10	15	20	50	mV
Thermal drift of gate-source voltage difference	$\left\|\dfrac{d\ \Delta V_{GS}}{dT}\right\|$	< 5	5	10	20	20	40	50	$\mu V/K$
Transfer conductance ratio	$\dfrac{g_{1fs}}{g_{2fs}}$	> 0,98 < 1,02	0,98 1,02	0,98 1,02	0,98 1,02	0,98 1,02	0,95 1,05	0,95 1,05	
Difference in transfer impedance [2]	$\left\|\Delta\dfrac{1}{g_{fs}}\right\|$	< 6	6	12	12	12	20	30	Ω
Difference in penetration factor [3]	$\left\|\Delta\dfrac{g_{os}}{g_{fs}}\right\|$	< 10	30	40	50	60	70	100	$\mu V/V$
Common mode rejection ratio [4]	CMRR	> 100	90	90	90	90	90	80	dB

[1]) Measured under pulse conditions.

[2]) The difference in transfer impedance is equal to the ratio of the change of the gate-source voltage difference to the change of drain current, at constant drain-gate voltage.
$(\Delta\dfrac{1}{g_{fs}} = \dfrac{d\ \Delta V_{GS}}{d\ I_D}$ at V_{DG} = constant)

[3]) The difference in penetration factor is equal to the ratio of the change of the gate-source voltage difference to the change of drain-gate voltage, at constant drain current.
$(\Delta\dfrac{g_{os}}{g_{fs}} = \dfrac{d\ \Delta V_{GS}}{d\ V_{DG}}$ at I_D = constant)

[4]) Common mode rejection ratio
CMRR (in dB) = $-20\log\left\|\Delta\dfrac{g_{os}}{g_{fs}}\right\|$

CHARACTERISTICS (Individual transistor) $T_{amb} = 25\ ^{\circ}C$ unless otherwise specified

Gate cut-off current

$-V_{GS} = 20$ V; $V_{DS} = 0$	$-I_{GSS}$	<	100	pA
$-V_{GS} = 20$ V; $V_{DS} = 0$; $T_{amb} = 125\ ^{\circ}C$	$-I_{GSS}$	<	20	nA

Gate current

$I_D = 200\ \mu A$; $V_{DG} = 15$ V; $T_{amb} = 125\ ^{\circ}C$	I_G	<	10	nA

Drain current

$V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}		0,5 to 10	mA [1])

Gate-source voltage

$I_D = 200\ \mu A$; $V_{DG} = 15$ V	$-V_{GS}$	<	2,7	V

Gate-source cut-off voltage

$I_D = 1$ nA; $V_{DG} = 15$ V	$-V_{(P)GS}$		0,5 to 3,5	V

Transfer conductance at f = 1 kHz

$I_D = 200\ \mu A$; $V_{DG} = 15$ V	g_{fs}	>	1,0	mS

Output conductance at f = 1 kHz

$I_D = 200\ \mu A$; $V_{DG} = 15$ V	g_{os}	<	5	μS

Input capacitance at f = 1 MHz

$I_D = 200\ \mu A$; $V_{DG} = 15$ V	C_{is}	<	8	pF [2])

Feedback capacitance at f = 1 MHz

$I_D = 200\ \mu A$; $V_{DG} = 15$ V	C_{rs}	<	1,0	pF [2])

Equivalent noise voltage

$I_D = 200\ \mu A$; $V_{DS} = 15$ V B = 0,6 to 100 Hz	V_n	<	0,5	μV

[1]) Measured under pulse conditions.
[2]) Measured with case grounded.

7Z67190

$-V_{GS} = 20\,V$
$V_{DS} = 0$

I_{GSS} (nA)

T_j (ºC)

typ

7Z67189

I_D (mA)

$V_{DS} = 15\,V$
$T_j = 25\,^oC$

typ. values
$T_j = 25\,^oC$

$V_{GS} = 0$

$-V_{GS} = 0,5\,V$

max

typ

1 V

min

$-V_{GS}$ (V)

V_{DS} (V)

7Z67191

$|y_{fs}|$ (mA/V)

typ. values
$V_{DS} = 15\,V$
$f = 1\,kHz$
$T_{amb} = 25\,^oC$

$I_{DSS} = 5\,mA$

$I_{DSS} = 10\,mA$

$I_{DSS} = 0,3\,mA$

I_D (mA)

7Z67187

typ. correlation between $-V_{(P)GS}$ and I_{DSS}

$-V_{(P)GS}$
(at $I_D = 1\,nA$)
(V)

$V_{DS} = 15\,V$
$T_j = 25\,^oC$

I_{DSS} at $V_{GS} = 0$ (mA)

7Z67186

$|y_{os}|$
($\mu A/V$)

typ. values
$I_D = 200\,\mu A$
$f = 1\,kHz$
$T_{amb} = 25\,^oC$

$I_{DSS} = 10\,mA$
$I_{DSS} = 5\,mA$
$I_{DSS} = 0,3\,mA$

V_{DS} (V)

7Z67192

$|y_{os}|$
($\mu A/V$)

typ. values
$V_{DS} = 15\,V$
$f = 1\,kHz$
$T_{amb} = 25\,^oC$

$I_{DSS} = 10\,mA$
$I_{DSS} = 5\,mA$
$I_{DSS} = 0,3\,mA$

I_D (mA)

7Z67188

$V_{DS} = 15\,V$
$T_{amb} = 25\ ^oC$
$f = 1\,MHz$
case grounded

C_{is} (pF)

typ

7Z67185

$V_{DS} = 15\,V$
$T_{amb} = 25\ ^oC$
$f = 1\,MHz$
case grounded

C_{rs} (pF)

typ

$-V_{GS}$ (V)

$-V_{GS}$ (V)

7Z67193

e_n

$(\frac{nV}{\sqrt{Hz}})$

$V_{DS} = 15\,V$
$I_D = 200\,\mu A$
$T_{amb} = 25\ ^oC$

typ

f (Hz)

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Planar epitaxial symmetrical junction field effect transistor in a microminiature plastic envelope. It is intended for low level general purpose amplifiers in thick and thin-film circuits.

QUICK REFERENCE DATA

			BFR30	BFR31	
Drain-source voltage	$\pm V_{DS}$	max.	25		V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25		V
Total power dissipation up to $T_{amb} = 65\,^oC$	P_{tot}	max.	250		mW
Drain current			BFR30	BFR31	
$V_{DS} = 10$ V; $V_{GS} = 0$	I_{DSS}	$>$	4	1	mA
		$<$	10	5	mA
Transfer admittance (common source)		$>$	1,0	1,5	mS
$I_D = 1$ mA; $V_{DS} = 10$ V; $f = 1$ kHz	$|Y_{fs}|$	$<$	4,0	4,5	mS

MECHANICAL DATA
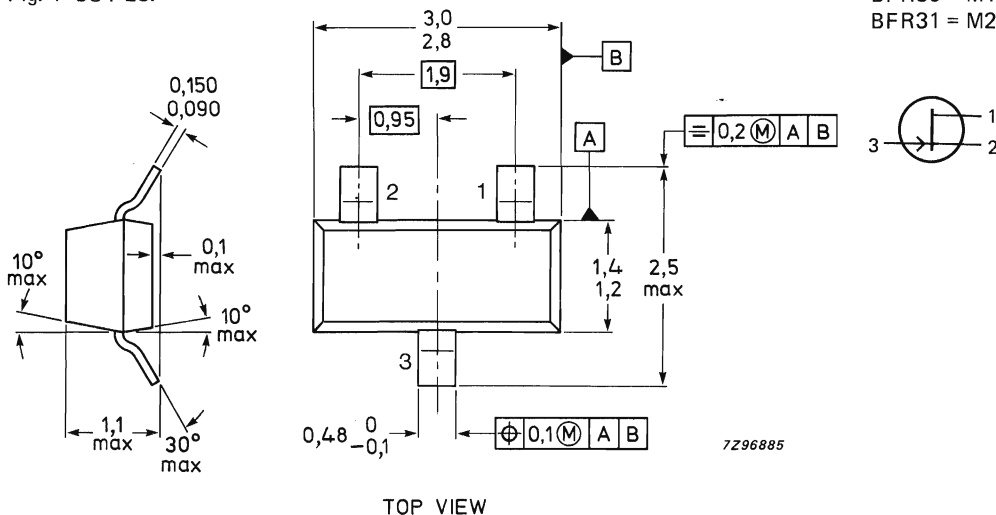
Dimensions in mm

Marking code

Fig. 1 SOT-23.

BFR30 = M1
BFR31 = M2

TOP VIEW

Note: Drain and source are interchangeable.

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage see Fig. 2	$\pm V_{DS}$	max.	25	V
Drain-gate voltage (open source) see Fig. 2	V_{DGO}	max.	25	V
Gate-source voltage (open drain) see Fig. 2	$-V_{GSO}$	max.	25	V
Drain current	I_D	max.	10	mA
Gate current	I_G	max.	5	mA
Total power dissipation up to $T_{amb} = 65\ ^oC$**	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}		−65 to + 175	^oC
Junction temperature	T_j	max.	175	^oC

THERMAL CHARACTERISTICS*

$$T_j = P \times (R_{th\ j\text{-}t} + R_{th\ t\text{-}s} + R_{th\ s\text{-}a}) + T_{amb}$$

Thermal resistance

From junction to tab	$R_{th\ j\text{-}t}$	=	60	K/W
From tab to soldering points	$R_{th\ t\text{-}s}$	=	280	K/W
From soldering points to ambient**	$R_{th\ s\text{-}a}$	=	90	K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

			BFR30	BFR31	
Gate cut-off current $-V_{GS} = 10\ V; V_{DS} = 0$	$-I_{GSS}$	<	0,2	0,2	nA
Drain current $V_{DS} = 10\ V; V_{GS} = 0$	I_{DSS}	> <	4 10	1 5	mA mA
Gate-source voltage $I_D = 1\ mA; V_{DS} = 10\ V$	$-V_{GS}$	> <	0,7 3,0	0 1,3	V V
$I_D = 50\ \mu A; V_{DS} = 10\ V$	$-V_{GS}$	<	4,0	2,0	V
Gate-source cut-off voltage $I_D = 0,5\ nA; V_{DS} = 10\ V$	$-V_{(P)GS}$	<	5	2,5	V

y parameters

			BFR30	BFR31	
Transfer admittance at f = 1 kHz; $T_{amb} = 25\ ^oC$ $I_D = 1\ mA; V_{DS} = 10\ V$	$|y_{fs}|$	> <	1,0 4,0	1,5 4,5	mS mS
$I_D = 200\ \mu A; V_{DS} = 10\ V$	$|y_{fs}|$	>	0,5	0,75	mS
Output admittance at f = 1 kHz $I_D = 1\ mA; V_{DS} = 10\ V$	$|y_{os}|$	<	40	25	μS
$I_D = 200\ \mu A; V_{DS} = 10\ V$	$|y_{os}|$	<	20	15	μS

* See *Thermal characteristics.*
** Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

y parameters (continued)

			BFR30	BFR31	
Input capacitance at f = 1 MHz					
I_D = 1 mA; V_{DS} = 10 V	C_{is}	<	4	4	pF
I_D = 200 μA; V_{DS} = 10 V	C_{is}	<	4	4	pF
Feedback capacitance at f = 1 MHz; T_{amb} = 25 °C					
I_D = 1 mA; V_{DS} = 10 V	C_{rs}	<	1,5	1,5	pF
I_D = 200 μA; V_{DS} = 10 V	C_{rs}	<	1,5	1,5	pF
Equivalent noise voltage					
I_D = 200 μA; V_{DS} = 10 V					
B = 0,6 to 100 Hz	V_n	<	0,5	0,5	μV
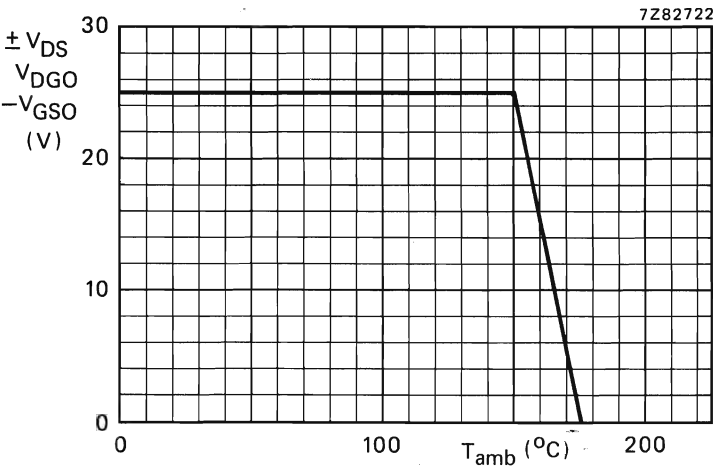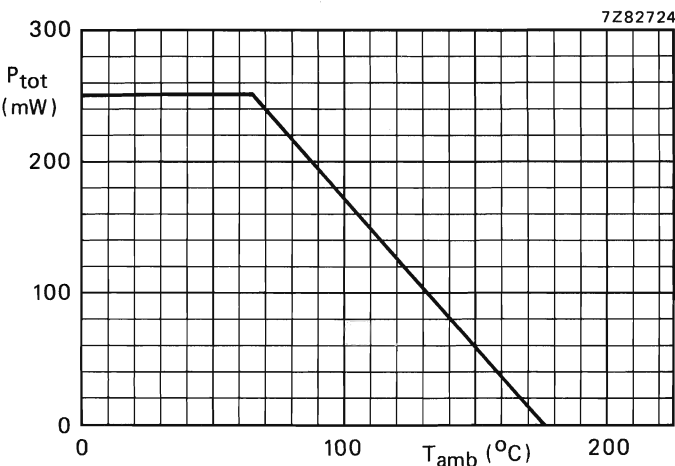
Fig. 2 Voltage derating curve.

Fig. 3 Power derating curve.

7Z62138.1

$-V_{GS} = 10V$
$V_{DS} = 0$

I_{GSS}
(nA)

10^3

10^2

10

1

10^{-1}

10^{-2}

10^{-3}

0   50   100   150 T_j (°C) 200

typ

Fig. 4.

Fig. 5.

Fig. 6.

Fig. 7.

Fig. 8.

Fig. 9.

7Z62139

|y_{fs}| (mA/V)

typical values
$V_{DS} = 10V$
$f = 1kHz$
$T_{amb} = 25°C$

BFR31

BFR30

I_D (mA)

Fig. 10.

7Z62140

|y_{os}| (μA/V)

typical values
$V_{DS} = 10V$
$f = 1kHz$
$T_{amb} = 25°C$

BFR30

BFR31

I_D (mA)

Fig. 11.

7Z62131

typical values
f=1kHz
$T_{amb}=25°C$

$|y_{os}|$
$(\mu A/V)$

10^4

10^3

10^2

$I_D=4mA$

1mA

BFR30

BFR31

10

0   10   20 $V_{DS}(V)$ 30

Fig. 12.

7Z62133

C_{is}
(pF)

7.5

5

2.5

0

typ

$V_{DS}=10V$
f = 1MHz
$T_{amb}=25°C$

0   2.5 $-V_{GS}$ (V)   5

Fig. 13.

7Z62132

$-C_{rs}$
(pF)

1.5

1

0.5

0

typ

$V_{DS}=10V$
f = 1MHz
$T_{amb}=25°C$

0   2.5 $-V_{GS}$ (V)   5
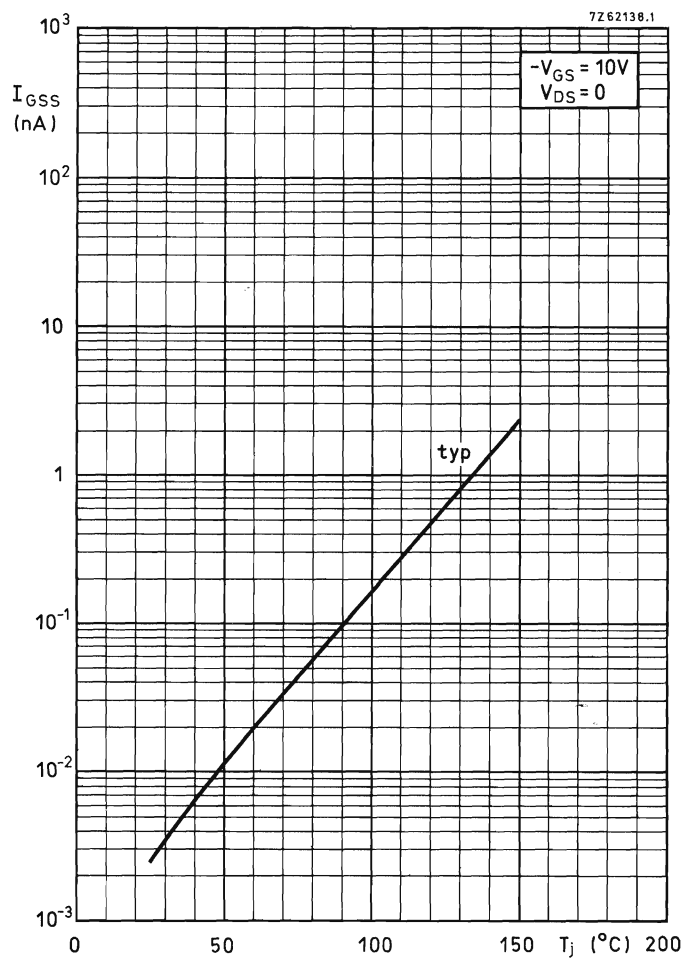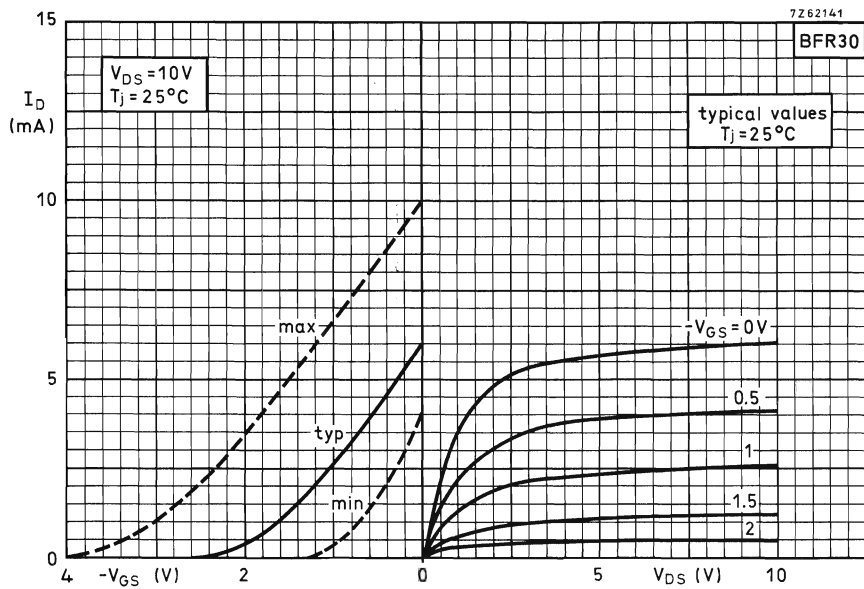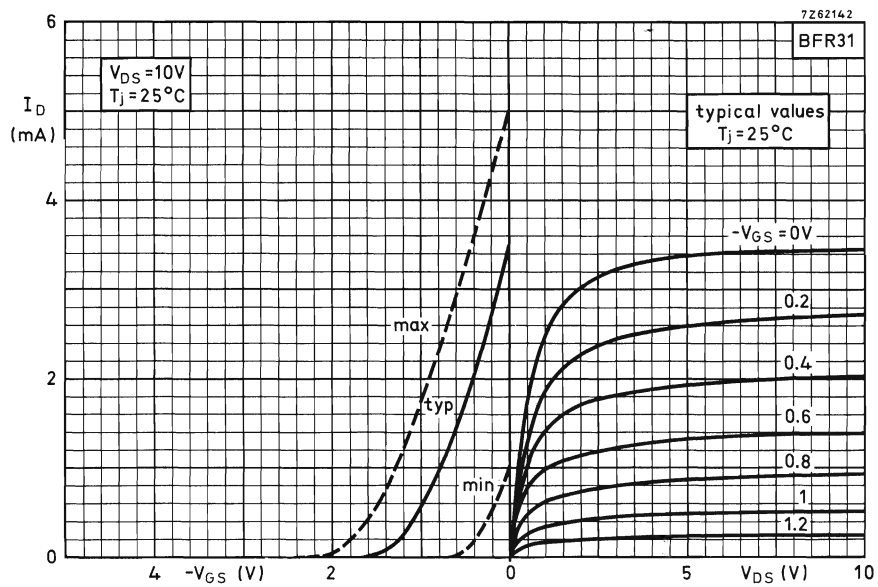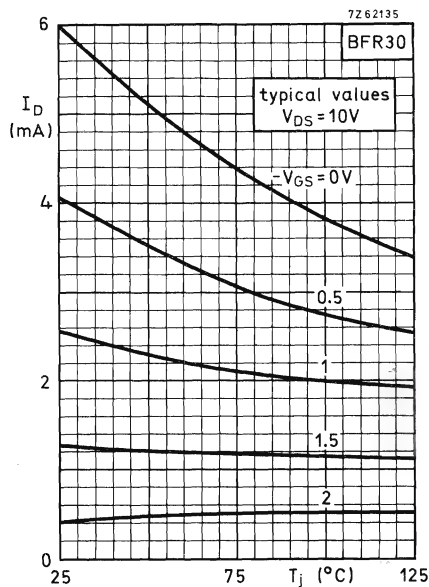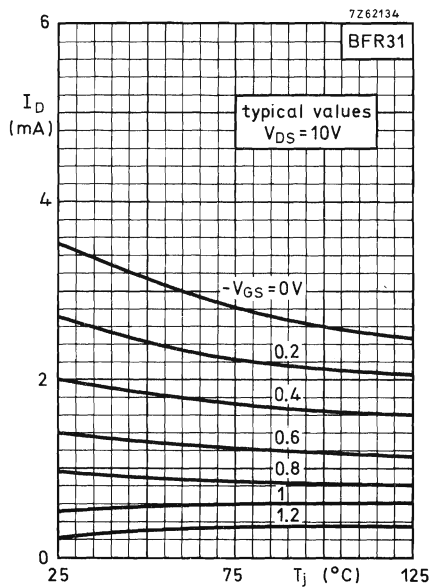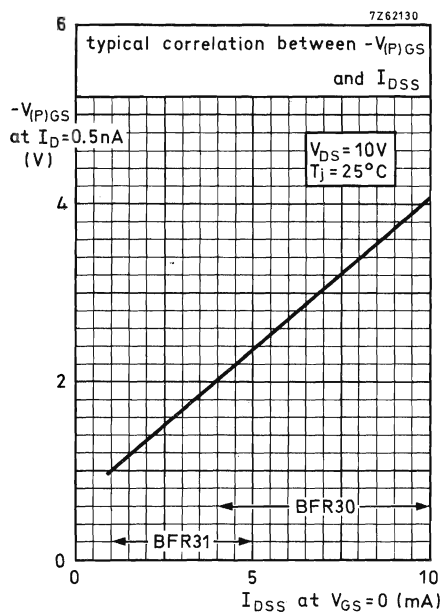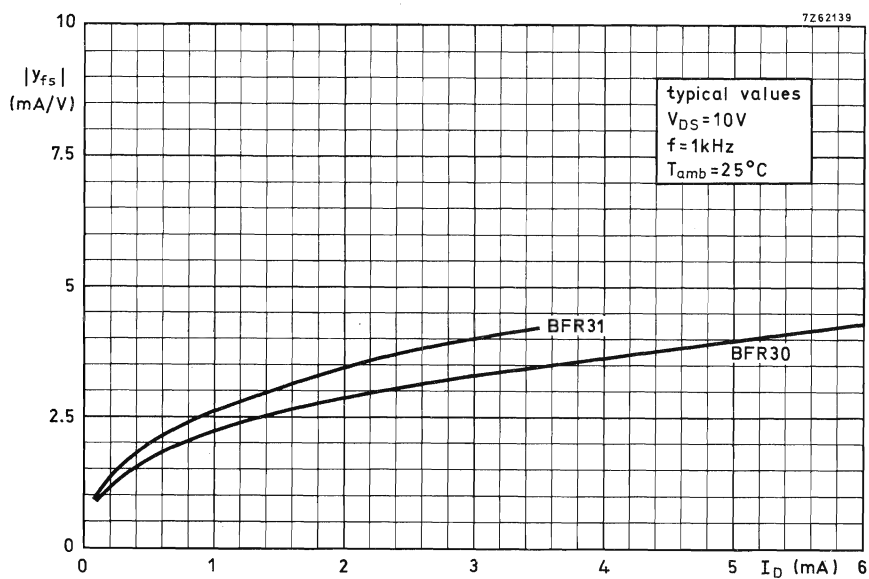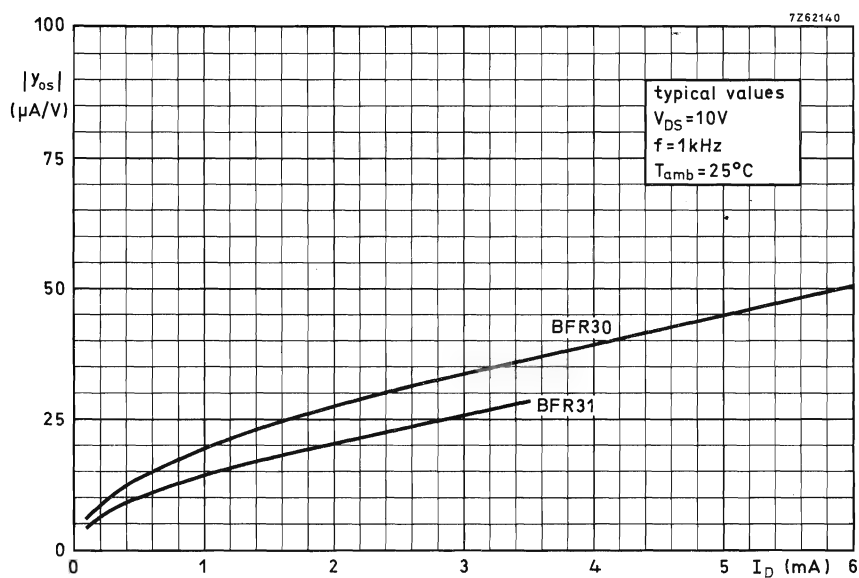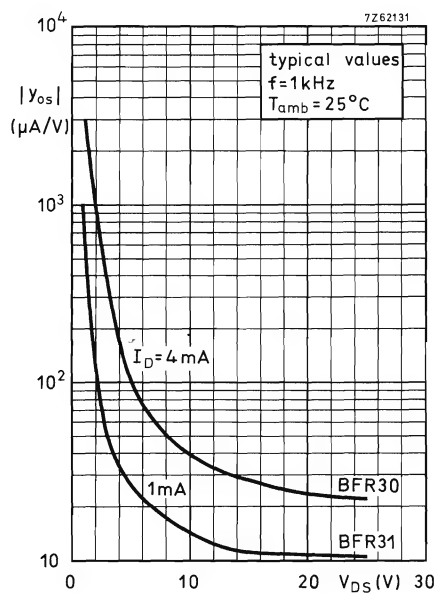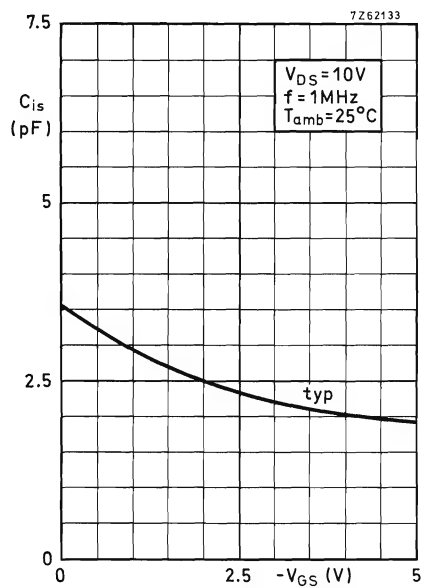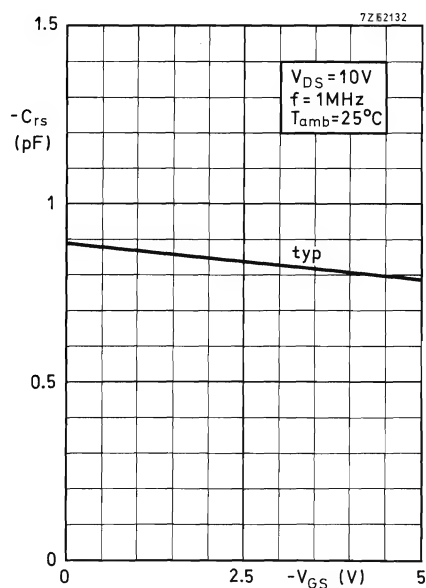
Fig. 14.
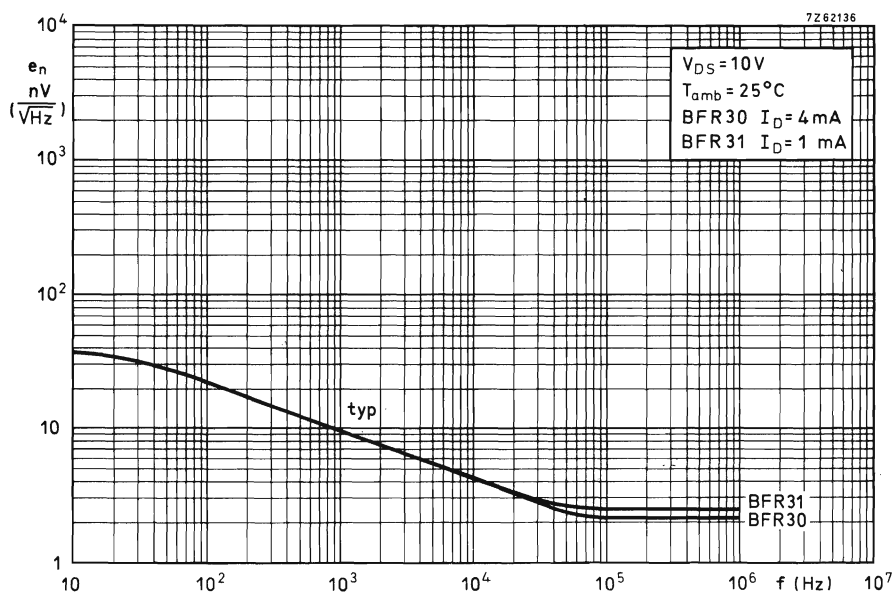
Fig. 15.
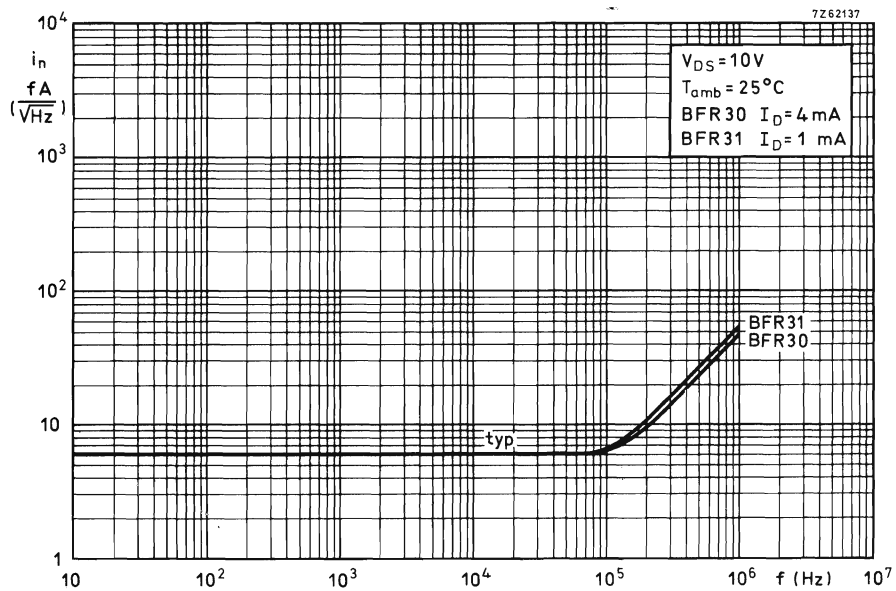
Fig. 16.

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR

Symmetrical n-channel silicon junction field-effect transistor, designed primarily for use as a source follower with the input protected against successive voltage surges by a forward and reverse integrated diode.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage (open drain)	$-V_{GS}$	max.	30	V
Total power dissipation up to $T_{amb} = 60\ ^{\circ}C$	P_{tot}	max.	200	mW
Drain current				
$V_{DS} = 6$ V; $V_{GS} = 0$: BFR101A	I_{DSS}		0,2 to 1,5	mA
$V_{DS} = 6$ V; $V_{GS} = 0$: BFR101B	I_{DSS}		1,0 to 5,0	mA
Transfer admittance (common source)				
$V_{DS} = 6$ V; $V_{GS} = 0$; f = 1 kHz: BFR101A	$\|y_{fs}\|$	$>$	1,2	mS
$V_{DS} = 6$ V; $V_{GS} = 0$; f = 1 kHz: BFR101B	$\|y_{fs}\|$	$>$	2,5	mS

MECHANICAL DATA   Dimensions in mm   **Marking code**

Fig. 1 SOT-143.   BFR101A = M97
                                                          BFR101B = M98

TOP VIEW

7Z85014.7

Note: Drain and source are interchangeable.

See also *Soldering recommendations*.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Drain current (d.c.)	I_D	max.	20	mA
Gate current (d.c.)	I_G	max.	10	mA
Total power dissipation up to $T_{amb} = 60\,^oC*$	P_{tot}	max.	200	mW
Storage temperature	T_{stg}		-65 to $+150$	^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\,j-a}$	=	460	K/W

CHARACTERISTICS with source connected to case for all measurements

$T_{amb} = 25\,^oC$ unless otherwise specified

		BFR101A	BFR101B	
Gate leakage current $V_{DS} = 6$ V; $I_D = 10\,\mu A$	$-I_G$	$<$ 5	5	nA
Drain current* $V_{DS} = 6$ V; $V_{GS} = 0$	I_{DSS}	0,2 to 1,5	1 to 5	mA
Gate-source cut-off voltage $V_{DS} = 6$ V; $I_D = 1\,\mu A$	$-V_{(P)GS}$	0,2 to 1	0,5 to 2,5	V
Small-signal common-source characteristics $V_{DS} = 6$ V; $V_{GS} = 0$				
Transfer admittance* f = 1 kHz	$|y_{fs}|$	$>$ 1,2	2,5	mS
Output admittance at f = 1 kHz**	$|y_{os}|$	typ. 10	50	mS
Input capacitance at f = 1 MHz diodes not connected	C_{is}	$<$ 5	5	pF
Diode capacitance $V_D = 0$; source and drain not connected	C_d	typ. 0,7	0,7	pF
Diode forward voltage $\pm I_F = 10$ mA	V_F	0,7 to 1,2	0,7 to 1,2	V

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.
** Measured under pulse conditions: $t_p = 100$ ms; $\delta \leqslant 0,1$.

MATCHED N-CHANNEL FETS

Matched pair of symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes, mounted together in a metal S-clip.

These devices are intended for low level differential amplifiers.

QUICK REFERENCE DATA

Characteristics measured at T_{amb} = 25 °C; I_D = 0,5 mA; V_{DG} = 15 V

			BFS21	BFS21A	
Gate cut-off current	I_G	<	0,5	0,5	nA
Gate -source voltage difference	$\|\Delta V_{GS}\|$	<	20	10	mV
Thermal drift of gate-source voltage difference	$\left\|\dfrac{d\Delta V_{GS}}{dT}\right\|$	<	75	40	μV/K
Difference in transfer impedance	$\left\|\Delta\dfrac{1}{g_{fs}}\right\|$	<	15	7,5	Ω
Difference in penetration factor	$\left\|\Delta\dfrac{g_{os}}{g_{fs}}\right\|$	<	1	0,5	mV/V
Common mode rejection ratio	CMRR	>	60	66	dB

MECHANICAL DATA
SOT-52 (see next page)

TOTAL DEVICE

Dimensions in mm

MECHANICAL DATA

SOT-52

7Z58607.2
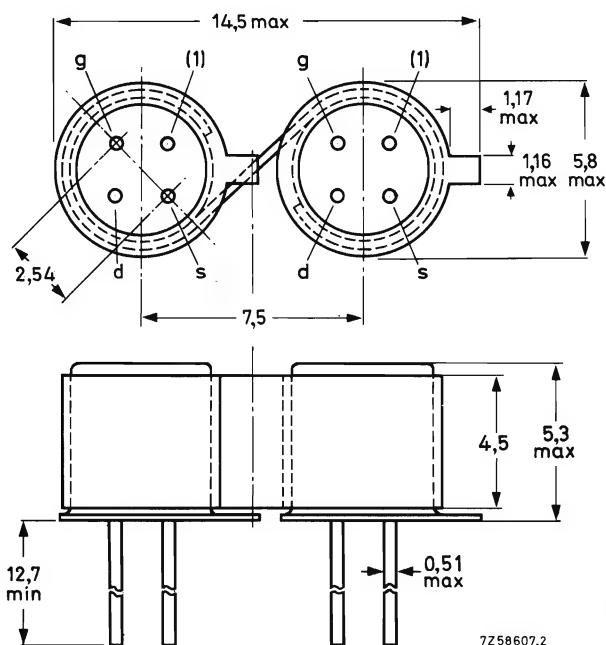
(1) = shield lead (connected to case).

Maximum lead diameter is guaranteed only for 12,7 mm.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage between any 2 terminals	V	max.	30	V
Drain current	I_D	max.	4	mA
Gate current	I_G	max.	0,5	mA
Total power dissipation up to T_{amb} = 100 ^oC	P_{tot}	max.	30	mW
Operating ambient temperature	T_{amb}	-20 to $+100$		^oC

CHARACTERISTICS (total device)

T_{amb} = 25 ^oC unless otherwise specified

			BFS21	BFS21A	
Drain current ratio					
V_{DG}= 15 V; V_{GS} = 0; T_j = 25 ^oC	$\dfrac{I_{D1}-S1S}{I_{D2}-S2S}$		$>$ 0,95 $<$ 1,05	0,95 1,05	
Gate-source voltage difference					
I_D = 500 μA; V_{DG} = 15 V	$\left\|\Delta V_{GS}\right\|$		$<$ 20	10	mV
I_D = 100 μA; V_{DG} = 15 V	$\left\|\Delta V_{GS}\right\|$		$<$ 20	10	mV
Thermal drift of gate-source voltage difference					
I_D = 500 μA; V_{DG} = 15 V	$\left\|\dfrac{d\ \Delta V_{GS}}{dT}\right\|$		$<$ 75	40	μV/K
I_D = 100 μA; V_{DG} = 15 V	$\left\|\dfrac{d\ \Delta V_{GS}}{dT}\right\|$		$<$ 75	40	μV/K

Change of gate-source voltage difference with ambient temperature

T_{amb} = 25 to 100 ^oC

			BFS21	BFS21A	
I_D = 500 μA; V_{DG} = 15 V	$\left\|\Delta V_{GS}(T_{amb2}) - \Delta V_{GS}(T_{amb1})\right\|$		$<$ 6	3	mV
I_D = 100 μA; V_{DG} = 15 V	$\left\|\Delta V_{GS}(T_{amb2}) - \Delta V_{GS}(T_{amb1})\right\|$		$<$ 6	3	mV
Difference of penetration factors [1])					
I_D = 500 μA; V_{DG} = 15 V	$\left\|\Delta \dfrac{gos}{gfs}\right\|$		$<$ 1	0,5	10^{-3}
I_D = 100 μA; V_{DG} = 15 V	$\left\|\Delta \dfrac{gos}{gfs}\right\|$		$<$ 1	0,5	10^{-3}
Difference of transfer impedances [2])					
I_D = 500 μA; V_{DG} = 15 V	$\left\|\Delta \dfrac{1}{gfs}\right\|$		$<$ 15	7,8	Ω
I_D = 100 μA; V_{DG} = 15 V	$\left\|\Delta \dfrac{1}{gfs}\right\|$		$<$ 75	37,5	Ω

[1]) The difference between the penetration factors is equal to the ratio of the change of the gate-source voltage difference to the change of drain-gate voltage, at constant drain current.

$$\left(\Delta \frac{gos}{gfs} = \frac{d\ \Delta V_{GS}}{d\ V_{DG}}\ \text{at } I_D = \text{constant}\right)$$

[2]) The difference between the transfer impedances is equal to the ratio of the change of the gate-source voltage difference to the change of drain current, at constant drain-gate voltage.

$$\left(\Delta \frac{1}{gfs} = \frac{d\ \Delta V_{GS}}{d\ I_D}\ \text{at } V_{DG} = \text{constant}\right)$$

CHARACTERISTICS (continued) (total device)

Common mode rejection ratio [1]			BFS21	BFS21A	
I_D = 500 μA; V_{DG} = 15 V	CMRR	>	60	66	dB
I_D = 100 μA; V_{DG} = 15 V	CMRR	>	60	66	dB

INDIVIDUAL TRANSISTOR

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Drain current	I_D	max.	20	mA
Gate current	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 25°	P_{tot}	max.	300	mW
Storage temperature	T_{stg}	−65 to +200		^{o}C
Junction temperature	T_j	max.	200	^{o}C

THERMAL RESISTANCE

From junction to ambient in free air (for individual transistor without S-clip)	$R_{th\ j-a}$	=	590	K/W

[1] Common mode rejection ratio

$$(CMRR)^{-1} = \Delta \frac{g_{os}}{g_{fs}} + \tfrac{1}{2} g_{cs} \Delta \frac{1}{g_{fs}}$$

where g_{cs} in this formula is the output conductance
of the summing current source.

The guaranteed values of CMRR apply at g_{cs} = 0.1 $\mu\Omega^{-1}$
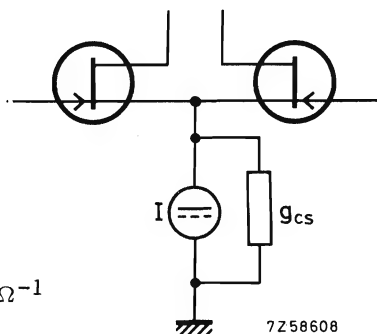
7Z58608

CHARACTERISTICS (individual transistor)

$T_{amb} = 25\,^{\circ}C$ unless otherwise specified

Gate cut-off current

$I_D = 500\ \mu A$; $V_{DS} = 15\ V$	I_G	<	0,5 nA
$I_D = 500\ \mu A$; $V_{DS} = 15\ V$; $T_{amb} = 100\ ^{\circ}C$	I_G	<	25 nA

Drain current

$V_{DS} = 15\ V$, $V_{GS} = 0$, $T_j = 25\ ^{\circ}C$	I_{DSS}	>	1 mA

Gate-source cut-off voltage

$I_D = 0.5\ nA$, $V_{DS} = 15\ V$	$-V_{(P)GS}$	<	6 V

Transfer conductance at f = 1 kHz

$I_D = 500\ \mu A$; $V_{DS} = 15\ V$	g_{fs}	>	1,0 mS

Output conductance at f = 1 kHz

$I_D = 500\ \mu A$; $V_{DS} = 15\ V$	g_{os}	<	15 μS

Input capacitance at f = 1 MHz

$I_D = 500\ \mu A$; $V_{DS} = 15\ V$	C_{is}	<	5 pF

Feedback capacitance at f = 1 MHz

$I_D = 500\ \mu A$; $V_{DS} = 15\ V$	C_{rs}	<	0,75 pF

Equivalent noise voltage

f = 10 Hz

$I_D = 500\ \mu A$; $V_{DS} = 15\ V$	$V_n/\sqrt{B}$	<	200 $nV/\sqrt{Hz}$
$V_{DS} = 15\ V$, $V_{GS} = 0$	$V_n/\sqrt{B}$	<	75 $nV/\sqrt{Hz}$

N-CHANNEL SILICON FET

Symmetrical n-channel silicon epitaxial planar junction field-effect transistor in a microminiature plastic envelope. The transistor is intended for low level general purpose amplifiers in thick and thin-film circuits.

QUICK REFERENCE DATA

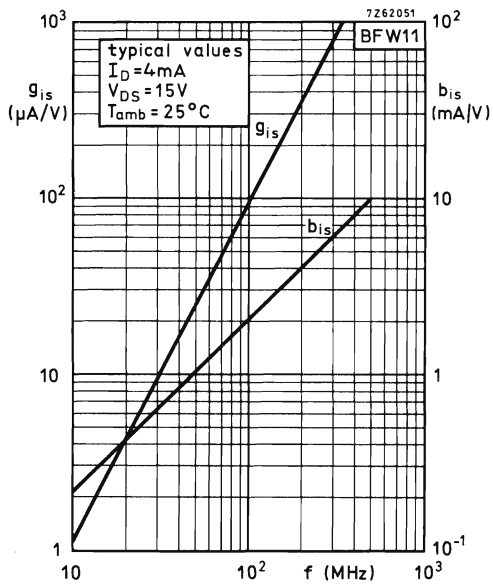|				
Drain-source voltage	$\pm V_{DS}$	max.	25	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25	V
Total power dissipation up to $T_{amb} = 65\ ^{o}C$	P_{tot}	max.	250	mW
Drain current $V_{DS} = 10$ V; $V_{GS} = 0$	I_{DSS}	$>$ $<$	0,2 1,5	mA mA
Transfer admittance (common source) $I_D = 0,2$ mA; $V_{DS} = 10$ V; f = 1 kHz	$|Y_{fs}|$	$>$	0,5	mS
Equivalent noise voltage $V_{DS} = 10$ V; $I_D = 200\ \mu A$; B = 0,6 to 100 Hz	V_n	$<$	0,5	μV

MECHANICAL DATA   Dimensions in mm   Marking code

Fig. 1 SOT-23.   BFT46 = M3

TOP VIEW

7Z96885

Note : Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Drain-gate voltage (open source)	V_{DGO}	max.	25	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25	V
Drain current	I_D	max.	10	mA
Gate current	I_G	max.	5	mA
Total power dissipation up to T_{amb} = 65 ^oC **	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}	-65 to +175		^oC
Junction temperature	T_j	max.	175	^oC

THERMAL CHARACTERISTICS*

$$R_{th\ j\text{-}t} + R_{th\ t\text{-}s} + R_{th\ s\text{-}a} = \frac{T_j - T_{amb}}{P}$$

Thermal resistance

From junction to tab	$R_{th\ j\text{-}t}$	=	60	K/W
From tab to soldering points	$R_{th\ t\text{-}s}$	=	280	K/W
From soldering points to ambient**	$R_{th\ s\text{-}a}$	=	90	K/W

CHARACTERISTICS

T_j = 25 ^oC unless otherwise specified

Gate cut-off current				
$-V_{GS}$ = 10 V; V_{DS} = 0	$-I_{GSS}$	<	0,2	nA
Drain current **				
V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	>	0,2	mA
		<	1,5	mA
Gate-source voltage				
I_D = 50 μA; V_{DS} = 10 V	$-V_{GS}$	>	0,1	V
		<	1,0	V
Gate-source cut-off voltage				
I_D = 0,5 nA; V_{DS} = 10 V	$-V_{(P)GS}$	<	1,2	V
y-parameters at f = 1 kHz;				
V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 ^oC				
Transfer admittance	$|y_{fs}|$	>	1,0	mS
Output admittance	$|y_{os}|$	<	10	μS
V_{DS} = 10 V; I_D = 200 μA;				
Transfer admittance	$|y_{fs}|$	>	0,5	mS
Output admittance	$|y_{os}|$	<	5	μS

* See *Thermal characteristics.*
** Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

Input capacitance at f = 1 MHz;
V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C $\qquad$ C_{is} $\qquad$ < $\qquad$ 5 pF

Feedback capacitance at f = 1 MHz;
V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C $\qquad$ C_{rs} $\qquad$ < $\qquad$ 1,5 pF

Equivalent noise voltage
V_{DS} = 10 V; I_D = 200 μA; T_{amb} = 25 °C
B = 0,6 to 100 Hz $\qquad$ V_n $\qquad$ < $\qquad$ 0,5 μV

Fig. 2 Voltage derating curve.

Fig. 3 Power derating curve.

7Z78216

Fig. 4 Typical values. $V_{DS} = 10$ V; $T_j = 25$ °C.

7Z78214

Fig. 5 Typical values. $V_{DS} = 10$ V.

7Z77642

Fig. 6 Correlation between $-V_{(P)GS}$ and I_{DSS}. $V_{DS} = 10$ V; $T_j = 25$ °C.

7Z77641A

Fig. 7.

7Z77640A
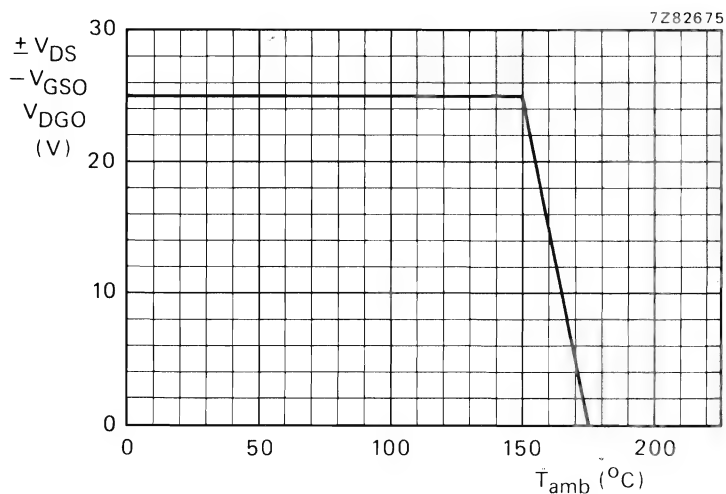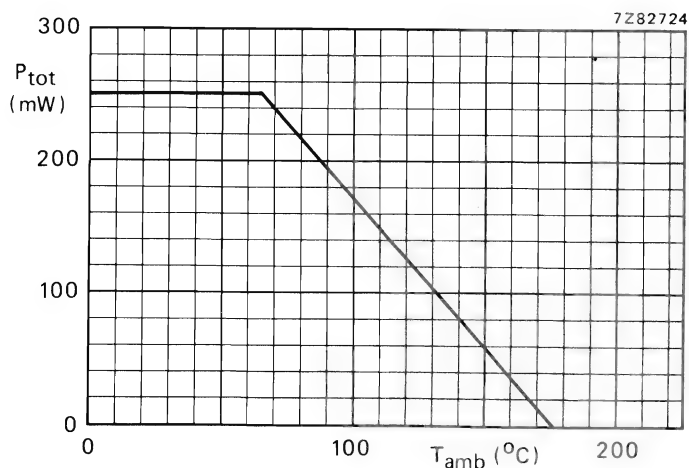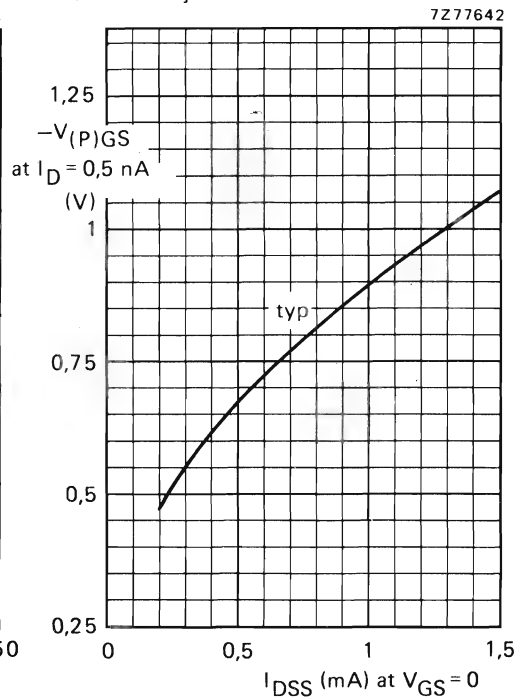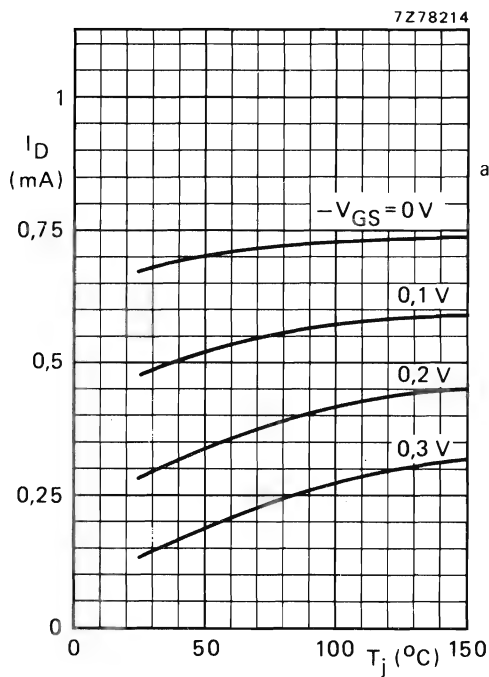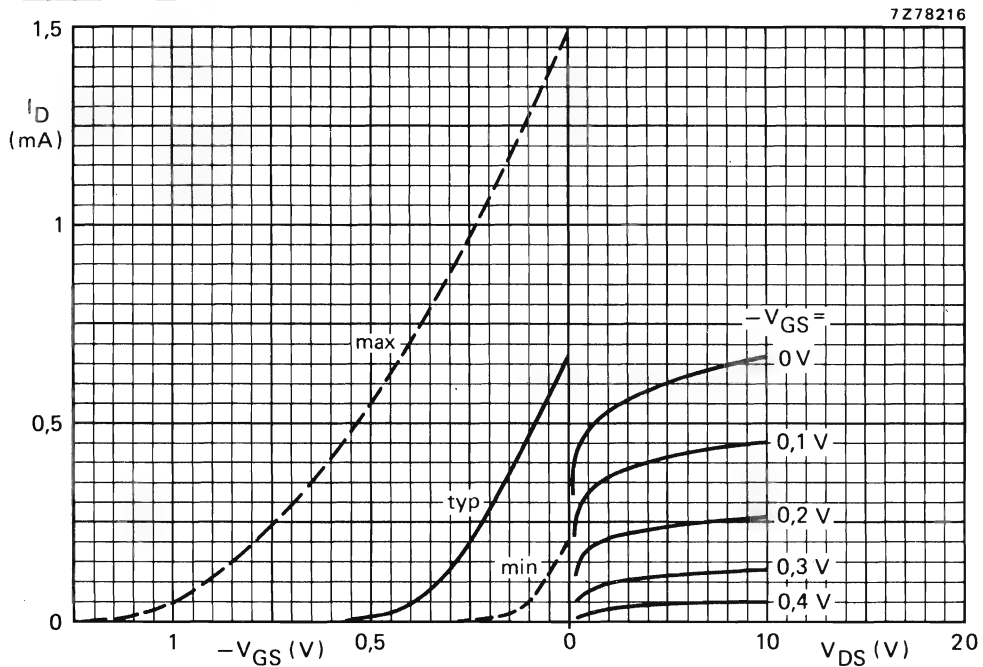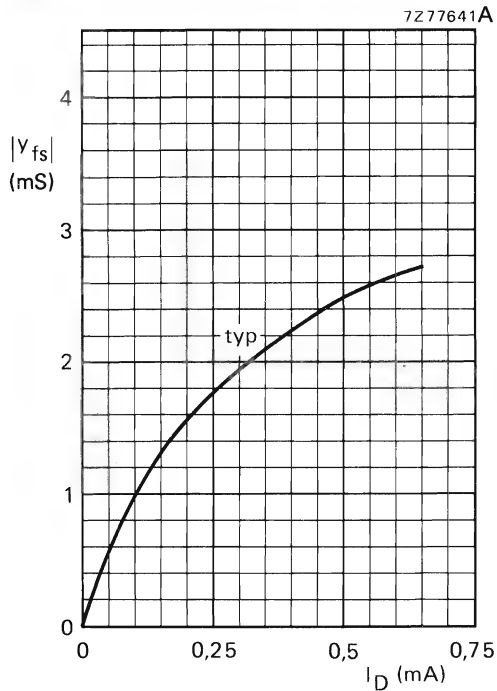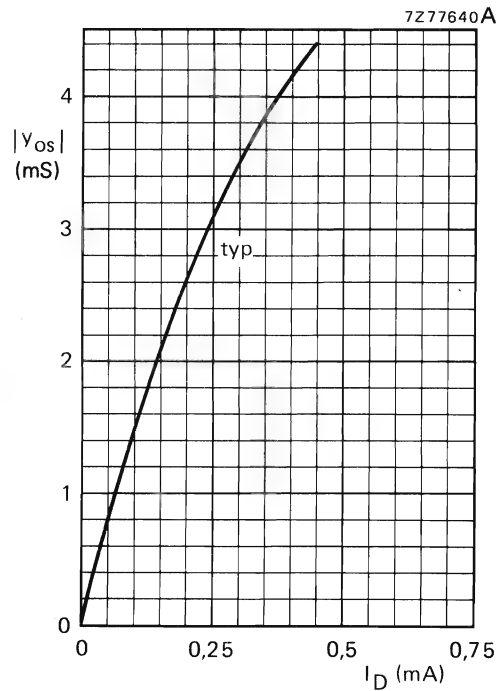
Fig. 8.

7Z77638
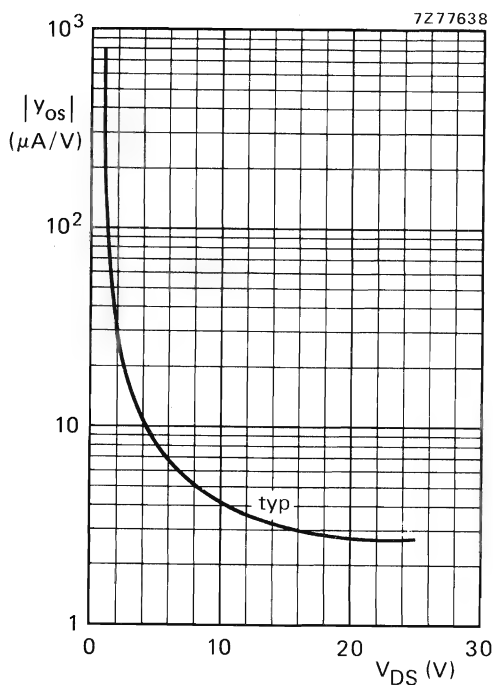
Fig. 9.

Fig. 7 $|y_{fs}|$ versus I_D.
$V_{DS} = 10$ V; f = 1 kHz; $T_{amb} = 25$ °C.

Fig. 8 $|y_{os}|$ versus I_D.
$V_{DS} = 10$ V; f = 1 kHz; $T_{amb} = 25$ °C.

Fig. 9 $|y_{os}|$ versus V_{DS}.
$I_D = 0,4$ mA; f = 1 kHz; $T_{amb} = 25$ °C.
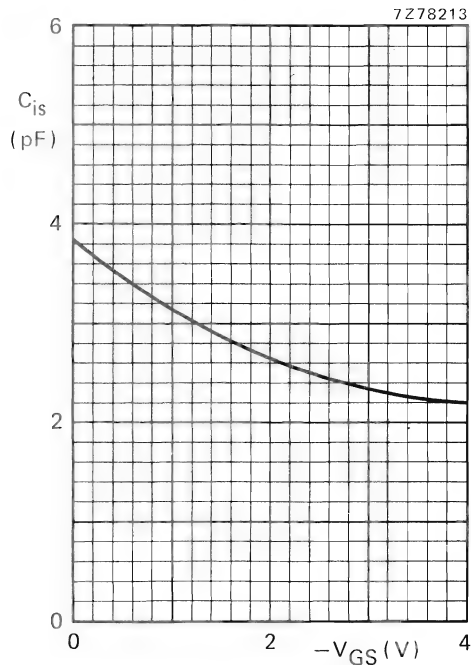
Fig. 10.
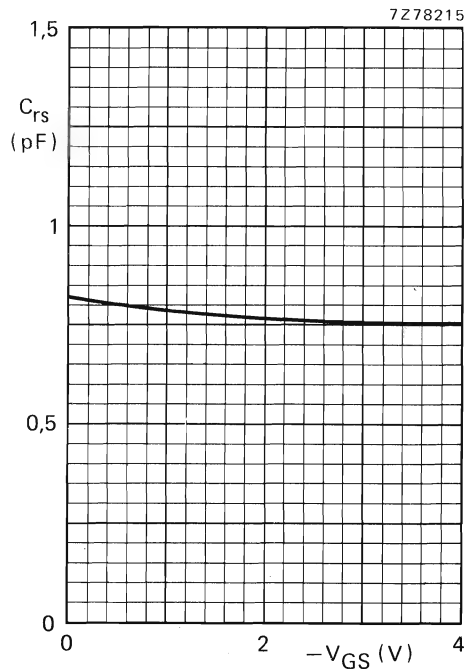
Fig. 11.
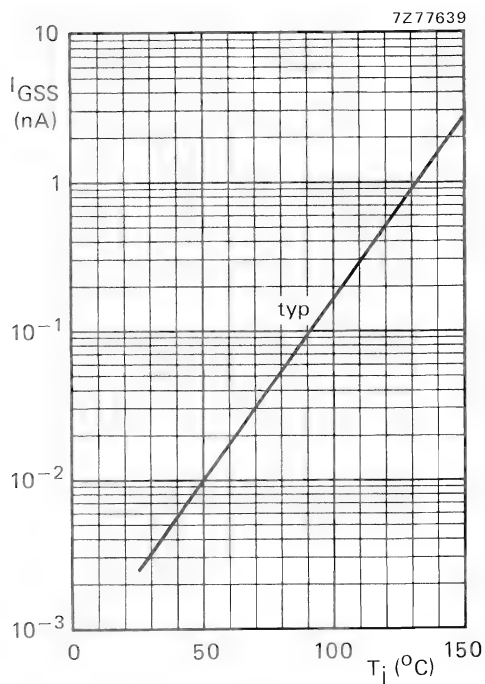
Fig. 12.

Fig.10 Typical values.
V_{DS} = 10 V, T_{amb} = 25 °C.

Fig.11 Typical values.
V_{DS} = 10 V, T_{amb} = 25 °C.

Fig.12 I_{GSS} versus T_j.
$-V_{GSS}$ = 10V; V_{DS} = 0.

7Z77644
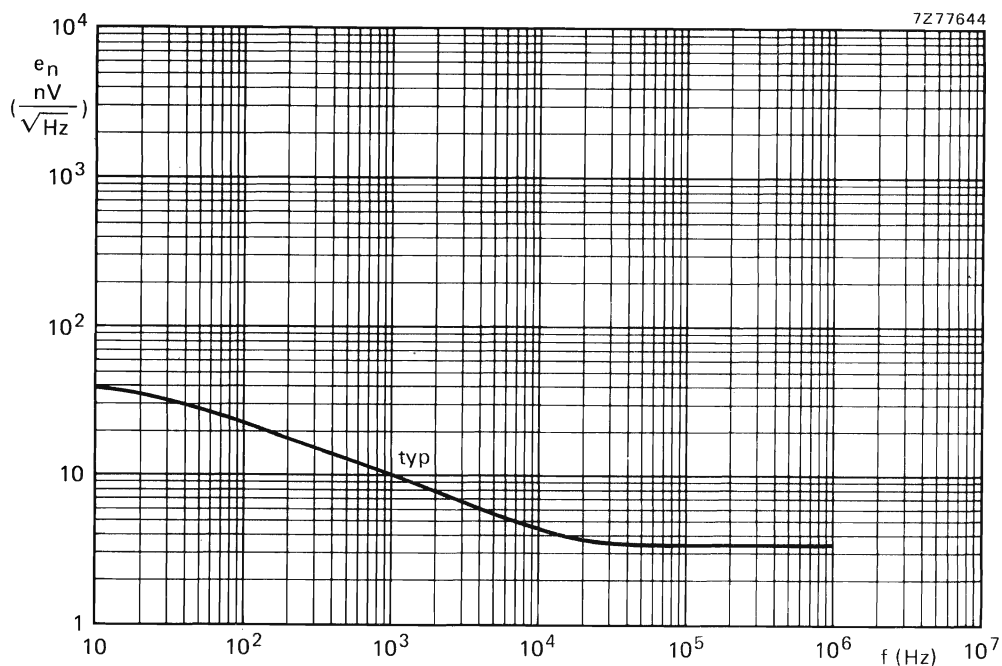
Fig. 13 V_{DS} = 10 V; I_D = 0,2 mA; T_{amb} = 25 °C.

7Z77643
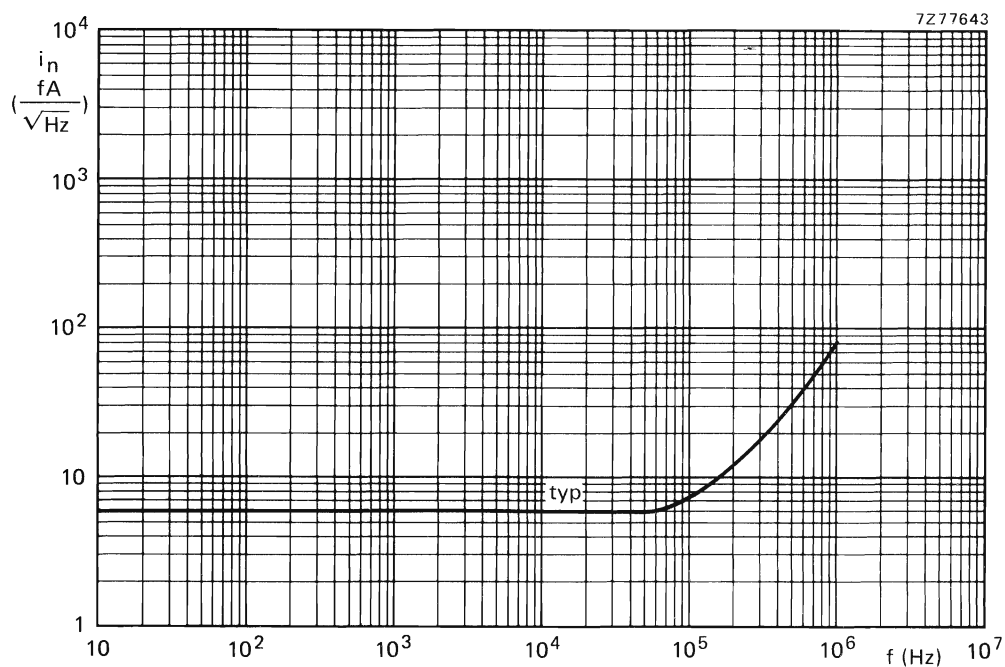
Fig. 14 V_{DS} = 10 V; I_D = 0,2 mA; T_{amb} = 25 °C.

N-CHANNEL SILICON FETS

Symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes with the shield lead connected to the case. The transistors are designed for broad band amplifiers (0 to 300 MHz). Their very low noise at low frequencies makes these devices very suitable for differential amplifiers, electro-medical and nuclear detector preamplifiers.

QUICK REFERENCE DATA

			BFW10	BFW11	
Drain-source voltage	$\pm V_{DS}$	max.	30		V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30		V
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	300		mW
Drain current $V_{DS} = 15\ V; V_{GS} = 0$	I_{DSS}	$>$	8	4	mA
		$<$	20	10	mA
Gate-source cut-off voltage $I_D = 0,5\ nA; V_{DS} = 15\ V$	$-V_{(P)GS}$	$<$	8	6	V
Feedback capacitance at f = 1 MHz $V_{DS} = 15\ V; V_{GS} = 0$	C_{rs}	$<$	0,80	0,80	pF
Transfer admittance (common source) $V_{DS} = 15\ V; V_{GS} = 0; f = 200\ MHz$	$\|y_{fs}\|$	$>$	3,2	3,2	mS
Noise figure at $V_{DS} = 15\ V; V_{GS} = 0$ f = 100 MHz; $R_G = 1\ k\Omega$	F	$<$	2,5	2,5	dB
Equivalent noise voltage f = 10 Hz	$V_n/\sqrt{B}$	$<$	75	75	$nV/\sqrt{Hz}$

MECHANICAL DATA   Dimensions in mm

Fig. 1 TO-72.

Note: Drain and source are interchangeable.

(1) = shield lead connected to case

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Drain current	I_D	max.	20	mA
Gate current	I_G	max.	10	mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	300	mW
Storage temperature	T_{stg}	-65 to $+200$		^oC
Junction temperature	T_j	max.	200	^oC

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	$=$	**590**	K/W

CHARACTERISTICS

T_j = 25 $^{\circ}$C unless otherwise specified

Gate cut-off currents			BFW10	BFW11	
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	0.1	0.1	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_j = 150 $^{\circ}$C	$-I_{GSS}$	<	0.5	0.5	μA
Drain current [1])					
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	8	4	mA
		<	20	10	mA
Gate-source voltage					
I_D = 400 μA; V_{DS} = 15 V	$-V_{GS}$	>	2.0		V
		<	7.5		V
I_D = 50 μA; V_{DS} = 15 V	$-V_{GS}$	>		1.25	V
		<		4.0	V
Gate-source cut-off voltage					
I_D = 0.5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	8	6	V
y parameters					
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 $^{\circ}$C					
f = 1 kHz Transfer admittance	$|y_{fs}|$	>	3.5	3.0	mS
		<	6.5	6.5	mS
Output admittance	$|y_{os}|$	<	85	50	μS
f = 1 MHz Input capacitance	C_{is}	typ.	4	4	pF
		<	5	5	pF
Feedback capacitance	$-C_{rs}$	typ.	0.6	0.6	pF
		<	0.80	0.80	pF
f = 200 MHz Transfer admittance	$|y_{fs}|$	>	3.2	3.2	mS
Input conductance	g_{is}	<	800	800	μS
Output conductance	g_{os}	<	200	100	μS
Noise figure at f = 100 MHz; R_G = 1 kΩ					
V_{DS} = 15 V; V_{GS} = 0 ; T_{amb} = 25 $^{\circ}$C input tuned to minimum noise	F	<	2.5	2.5	dB
Equivalent noise voltage					
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25°C					
f = 10 Hz	$V_n/\sqrt{B}$	<	75	75	nV/$\sqrt{Hz}$

---

[1]) Measured under pulsed conditions.

7Z08477

BFW10

$V_{DS} = 15V$
$T_j = 25°C$

I_D (mA)

typical values

$-V_{GS} = 0$

1V

2V

3V

max

typ

min

$-V_{GS}(V)$ $V_{DS}(V)$

7Z08476

BFW11

$V_{DS} = 15V$
$T_j = 25°C$

I_D (mA)

typical values

$-V_{GS} = 0$

0.5V

1V

1.5V

2V

max

typ

min

$-V_{GS}(V)$ $V_{DS}(V)$

7Z08475

$V_{DS} = 15V$ typical values — BFW10

I_D (mA)

$-V_{GS} = 0$

$1V$

$2V$

T_j (°C)

7Z08474

$V_{DS} = 15V$ typical values — BFW11

I_D (mA)

$-V_{GS} = 0$

$0.5V$

$1V$

T_j (°C)

7Z62067

typical correlation between $-V_{(P)GS}$ and I_{DSS}

$-V_{(P)GS}$ at $I_D = 0.5nA$ (V)

$V_{DS} = 15V$
$T_j = 25°C$

BFW10

BFW11

I_{DSS} at $V_{GS} = 0$ (mA)

7Z62070

|y_fs| (mA/V)

typical values
$V_{DS} = 15V$
$f = 1kHz$
$T_{amb} = 25°C$

BFW11

BFW10

I_D (mA)

7Z62071

|y_os| (μA/V)

typical values
$V_{DS} = 15V$
$f = 1kHz$
$T_{amb} = 25°C$

BFW10

BFW11

I_D (mA)

Top left graph — 7Z62049 — BFW10:
typical values
$I_D = 8\,mA$
$V_{DS} = 15\,V$
$T_{amb} = 25°C$
g_{is} ($\mu A/V$), b_{is} (mA/V) vs f (MHz)
curves: g_{is}, b_{is}

Top right graph — 7Z62048 — BFW10:
typical values
$I_D = 8\,mA$
$V_{DS} = 15\,V$
$T_{amb} = 25°C$
b_{rs} ($\mu A/V$), $-C_{rs}$ (pF) vs f (MHz)
curves: b_{rs}, $-C_{rs}$

Bottom left graph — 7Z62047 — BFW10:
typical values
$I_D = 8\,mA$
$V_{DS} = 15\,V$
$T_{amb} = 25°C$
g_{fs}, $-b_{fs}$ (mA/V) vs f (MHz)
curves: g_{fs}, $-b_{fs}$

Bottom right graph — 7Z62046 — BFW10:
typical values
$I_D = 8\,mA$
$V_{DS} = 15\,V$
$T_{amb} = 25°C$
g_{os} ($\mu A/V$), b_{os} (mA/V) vs f (MHz)
curves: b_{os}, g_{os}

7Z62117.1

e_n
$\frac{nV}{\sqrt{Hz}}$ ( )

$V_{DS} = 15V$
$T_{amb} = 25°C$
BFW10 $I_D = 8$ mA
BFW11 $I_D = 4$ mA

typ

BFW11
BFW10

f (Hz)

7Z62115.1

i_n
$\frac{fA}{\sqrt{Hz}}$ ( )

$V_{DS} = 15V$
$T_{amb} = 25°C$
BFW10 $I_D = 8$ mA
BFW11 $I_D = 4$ mA

BFW11
BFW10

typ

f (Hz)

N-CHANNEL SILICON FETS

Symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes with the shield lead connected to the case. The transistors are intended for battery powered equipment and other low current-low voltage applications.

QUICK REFERENCE DATA

			BFW12	BFW13	
Drain-source voltage	$\pm V_{DS}$	max.	30		V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30		V
Total power dissipation up to T_{amb} = 110 ^{o}C	P_{tot}	max.	150		mW
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	$>$ $<$	1 5	0,2 1,5	mA mA
Gate-source cut-off voltage I_D = 0,5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	$<$	2,5	1,2	V
Feedback capacitance at f = 1 MHz V_{DS} = 15 V; V_{GS} = 0	C_{rs}	$<$	0,80	0,80	pF
Transfer admittance (common source) V_{DS} = 15 V; I_D = 200 μA; f = 1 kHz	$\lvert y_{fs} \rvert$	$>$	0,5	0,5	mS
Equivalent noise voltage V_{DS} = 15 V; I_D = 200 μA B = 0,6 to 100 Hz	V_n	$<$	0,5	0,5	μV

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.

Note: Drain and source are interchangeable.

(1) = shield lead connected to case

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Drain current	I_D	max.	10	mA
Gate current	I_G	max.	5	mA
Total power dissipation up to $T_{amb} = 110\ ^{o}C$	P_{tot}	max.	150	mW
Storage temperature	T_{stg}	-65 to $+200$		^{o}C
Junction temperature	T_j	max.	200	^{o}C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	**590**	K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Gate cut-off currents			BFW12	BFW13	
$-V_{GS} = 10$ V; $V_{DS} = 0$	$-I_{GSS}$	<	0.1	0.1	nA
$-V_{GS} = 10$ V; $V_{DS} = 0$; $T_j = 150\ ^oC$	$-I_{GSS}$	<	0.1	0.1	μA
Drain current [1])					
$V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}	>	1	0.2	mA
		<	5	1.5	mA
Gate-source voltage					
$I_D = 50\ \mu A$; $V_{DS} = 15$ V	$-V_{GS}$	>	0.5	0.1	V
		<	2.0	1.0	V
Gate-source cut-off voltage					
$I_D = 0.5$ nA; $V_{DS} = 15$ V	$-V_{(P)GS}$	<	2.5	1.2	V
y parameters at $f = 1$ kHz; $T_{amb} = 25\ ^oC$					
$V_{DS} = 15$ V; $V_{GS} = 0$					
Transfer admittance	$\|y_{fs}\|$	>	2.0	1.0	mS
Output admittance	$\|y_{os}\|$	<	30	10	μS
$V_{DS} = 15$ V; $I_D = 500\ \mu A$					
Transfer admittance	$\|y_{fs}\|$	>	1.5	–	mS
Output admittance	$\|y_{os}\|$	<	10	–	μS
$V_{DS} = 15$ V; $I_D = 200\ \mu A$					
Transfer admittance	$\|y_{fs}\|$	>	0.5	0.5	mS
Output admittance	$\|y_{os}\|$	<	5	5	μS
$f = 1$ MHz; $T_{amb} = 25\ ^oC$					
$V_{DS} = 15$ V; $V_{GS} = 0$					
Input capacitance	C_{iss}	<	5	5	pF
Feedback capacitance	$-C_{rs}$	<	0.80	0.80	pF
Equivalent noise voltage					
$V_{DS} = 15$ V; $I_D = 200\ \mu A$; $T_{amb} = 25\ ^oC$ $B = 0.6$ to 100 Hz	V_n	<	0.5	0.5	μV

---

[1]) Measured under pulsed conditions.

7Z62054

BFW12

$V_{DS} = 15V$
$T_j = 25°C$

typical values

I_D (mA)

max

typ

min

$-V_{GS} = 0V$

0.2

0.4

0.6

0.8

$-V_{GS}$ (V)

V_{DS} (V)

7Z62055

BFW13

$V_{DS} = 15V$
$T_j = 25°C$

typical values

I_D (mA)

max

typ

min

$-V_{GS} = 0V$

0.1

0.2

0.3

0.4

$-V_{GS}$ (V)

V_{DS} (V)

7Z62057

BFW12

typical values
$V_{DS} = 15V$

I_D (mA)

$-V_{GS} = 0V$

0.2

0.4

0.6

T_j (°C)

7Z62056

BFW13

typical values
$V_{DS} = 15V$

I_D (mA)

$-V_{GS} = 0V$

0.1

0.2

0.3

T_j (°C)

7Z62058

typical correlation between $-V_{(P)GS}$
and I_{DSS}

$-V_{(P)GS}$
at $I_D = 0.5nA$
(V)

$V_{DS} = 15V$

$T_j = 25°C$

BFW12

BFW13

I_{DSS} at $V_{GS} = 0$ (mA)

7Z62061

Graph showing |y_fs| (mA/V) versus I_D (mA) with curves for BFW12 and BFW13.

typical values
$V_{DS} = 15V$
$f = 1 kHz$
$T_{amb} = 25°C$

7Z62062

Graph showing |y_os| (µA/V) versus I_D (mA) with curves for BFW12 and BFW13.

typical values
$V_{DS} = 15V$
$f = 1 kHz$
$T_{amb} = 25°C$

7Z62118.1

$V_{DS} = 15V$
$T_{amb} = 25°C$
BFW12 $I_D = 1$ mA
BFW13 $I_D = 0.2$ mA

typ

BFW13
BFW12

7Z62116.1

$V_{DS} = 15V$
$T_{amb} = 25°C$
BFW12 $I_D = 1$ mA
BFW13 $I_D = 0.2$ mA

BFW13
BFW12

typ

N-CHANNEL SILICON FET

Symmetrical n-channel silicon planar epitaxial junction field-effect transistor in a TO-72 metal envelope with the shield lead connected to the case. The transistor is designed for general purpose amplifiers.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25	V
Total power dissipation up to $T_{amb} = 25\ ^{o}C$	P_{tot}	max.	300	mW
Drain current $V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}		2 to 20	mA
Gate-source cut-off voltage $I_D = 1,0$ nA; $V_{DS} = 15$ V	$-V_{(P)GS}$	$<$	8	V
Feedback capacitance at $f = 1$ MHz $V_{DS} = 15$ V; $V_{GS} = 0$	C_{rs}	$<$	2,0	pF
Transfer admittance (common source) $V_{DS} = 15$ V; $V_{GS} = 0$; $f = 10$ MHz	$|y_{fs}|$	$>$	1,6	mS

MECHANICAL DATA   Dimensions in mm

Fig. 1 TO-72.

(1) = shield lead connected to case

Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Drain-gate voltage (open source)	V_{DGO}	max.	25	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25	V
Drain current	I_D	max.	20	mA
Gate current	I_G	max.	10	mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	300	mW
Storage temperature	T_{stg}		-65 to $+200$	^oC
Junction temperature	T_j	max.	200	^oC

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	590	K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Gate cut-off currents				
$-V_{GS} = 20$ V; $V_{DS} = 0$	$-I_{GSS}$	<	1,0	nA
$-V_{GS} = 20$ V; $V_{DS} = 0$; $T_j = 150\ ^oC$	$-I_{GSS}$	<	1,0	μA
Drain current*				
$V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}		2 to 20	mA
Gate-source voltage				
$I_D = 200\ \mu$A; $V_{DS} = 15$ V	$-V_{GS}$		0,5 to 7,5	V
Gate-source cut-off voltage				
$I_D = 1,0$ nA; $V_{DS} = 15$ V	$-V_{(P)GS}$	<	8	V
y-parameters (common source)				
$V_{DS} = 15$ V; $V_{GS} = 0$				
Transfer admittance at f = 1 kHz	$|y_{fs}|$		2,0 to 6,5	mS
at f = 10 MHz		>	1,6	mS
Output admittance at f = 1 kHz	$|y_{os}|$	<	85	μS
Input capacitance at f = 1 MHz	C_{is}	<	6	pF
Feedback capacitance at f = 1 MHz	C_{rs}	<	2,0	pF

* Measured under pulse conditions.

P-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Silicon symmetrical P-channel junction FETs in a plastic TO-92 envelope and intended for application with analog switches, choppers, commutators etc.

A special feature is the interchangeability of the drain and source connections.

QUICK REFERENCE DATA

			BSJ174	BSJ175	BSJ176	BSJ177	
Drain-source voltage	$\pm V_{DS}$	max.	30				V
Gate-source voltage	V_{GSO}	max.	30				V
Gate current	$-I_G$	max.	50				mA
Total power dissipation up to $T_{amb} = 50\ ^\circ C$	P_{tot}	max.	400				mW
Drain current $-V_{DS} = 15$ V; $V_{GS} = 0$	$-I_{DSS}$	$>$	20	7	2	1,5	mA
		$<$	135	70	35	20	mA
Drain-source ON-resistance $-V_{DS} = 0,1$ V; $V_{GS} = 0$	$R_{DS\,on}$	$<$	85	125	250	300	Ω

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92.

Pinning:
1 = Source
2 = Gate
3 = Drain

diameter within 2,0 max is uncontrolled

7Z78972.3

Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	V_{GSO}	max.	30	V
Gate-drain voltage	V_{GDO}	max.	30	V
Gate current (d.c.)	$-I_G$	max.	50	mA
Total power dissipation up to $T_{amb} = 50\ ^oC$	P_{tot}	max.	400	mW
Storage temperature range	T_{stg}		-65 to $+150$	^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250	K/W

STATIC CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

				BSJ174	BSJ175	BSJ176	BSJ177	
Gate cut-off current $-V_{GS} = 20$ V; $V_{DS} = 0$	I_{GSS}	<		1	1	1	1	nA
Drain cut-off current $-V_{DS} = 15$ V; $-V_{GS} = 10$ V	$-I_{DSX}$	<		1	1	1	1	nA
Drain current $-V_{DS} = 15$ V; $V_{GS} = 0$	$-I_{DSS}$	>		20	7	2	1,5	mA
		<		135	70	35	20	mA
Gate-source breakdown voltage $I_G = 1\ \mu A$; $V_{DS} = 0$	$V_{(BR)GSS}$	>		30	30	30	30	V
Gate-source cut-off voltage $-I_D = 10$ nA; $V_{DS} = 0$	$V_{GS\ off}$	>		5	3	1	0,8	V
		<		10	6	4	2,25	V
Drain-source ON-resistance $-V_{DS} = 0,1$ V; $V_{GS} = 0$	R_{DSon}	<		85	125	250	300	Ω

DYNAMIC CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Input capacitance, f = 1 MHz

$-V_{GS} = 10\ V; V_{DS} = 0\ V$	C_{is}	typ.	8	pF
$-V_{GS} = V_{DS} = 0$	C_{is}	typ.	30	pF

Feedback capacitance, f = 1 MHz

$-V_{GS} = 10\ V; V_{DS} = 0\ V$	C_{rs}	typ.	4	pF

Switching times (see Fig. 2 + 3)			BSJ174	BSJ175	BSJ176	BSJ177	
Delay time	t_d	typ.	2	5	15	20	ns
Rise time	t_r	typ.	5	10	20	25	ns
Turn-on time	t_{on}	typ.	7	15	35	45	ns
Storage time	t_s	typ.	5	10	15	20	ns
Fall time	t_f	typ.	10	20	20	25	ns
Turn-off time	t_{off}	typ.	15	30	35	45	ns
Test conditions:	$-V_{DD}$		10	6	6	6	V
	$V_{GS\,off}$		12	8	6	3	V
	R_L		560	1200	2000	2900	Ω
	$V_{GS\,on}$		0	0	0	0	V

Fig. 2 Switching times test circuit
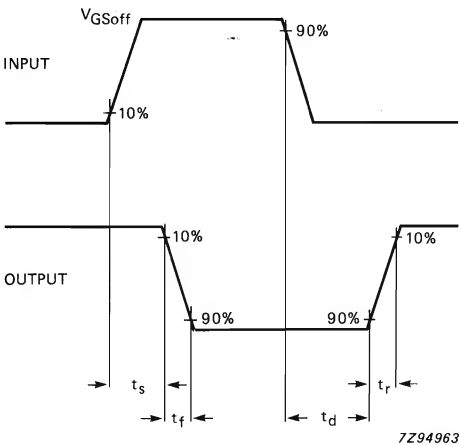
Fig. 3 Input and output waveforms
$t_d + t_r = t_{on}$
$t_s + t_f = t_{off}$

N-CHANNEL FETS

Silicon n-channel depletion type junction field-effect transistors in a plastic microminiature envelope intended for application in thick and thin-film circuits. The transistors are intended for low-power, chopper or switching applications in industrial service.

QUICK REFERENCE DATA

			BSR56	BSR57	BSR58	
Drain-source voltage	$\pm V_{DS}$	max.	40	40	40	V
Total power dissipation up to $T_{amb} = 65\ ^oC$	P_{tot}	max.	250	250	250	mW
Drain current $V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}	$>$	50	20	8	mA
		$<$	–	100	80	mA
Gate-source cut-off voltage $V_{DS} = 15$ V; $I_D = 0,5$ nA	$-V_{(P)GS}$	$>$	4	2	0,8	V
		$<$	10	6	4	V
Drain-source resistance (on) at f = 1 kHz $I_D = 0$; $V_{GS} = 0$	$r_{ds\ on}$	$<$	25	40	60	Ω
Feedback capacitance at f = 1 MHz $-V_{GS} = 10$ V; $V_{DS} = 0$	C_{rs}	$<$	5	5	5	pF
Turn-off time $V_{DD} = 10$ V; $V_{GS} = 0$						
$I_D = 20$ mA; $-V_{GSM} = 10$ V	t_{off}	$<$	25	–	–	ns
$I_D = 10$ mA; $-V_{GSM} = 6$ V	t_{off}	$<$	–	50	–	ns
$I_D = 5$ mA; $-V_{GSM} = 4$ V	t_{off}	$<$	–	–	100	ns

MECHANICAL DATA

Fig. 1 SOT-23.

Dimensions in mm

TOP VIEW

7Z96885
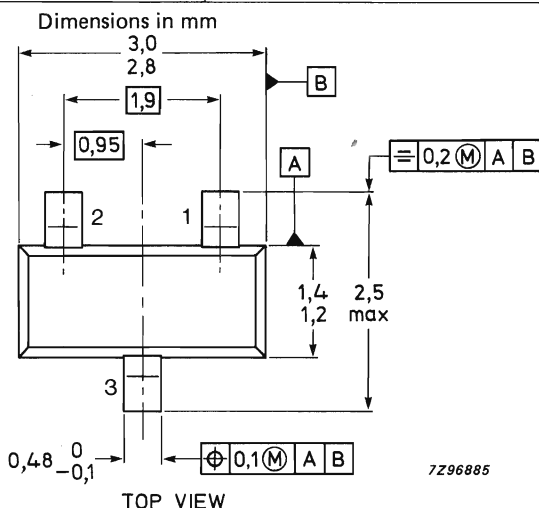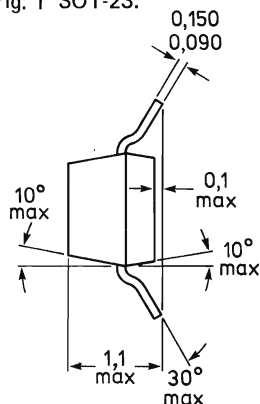
Marking code

BSR56 = M4
BSR57 = M5
BSR58 = M6

Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage (See Fig. 4)	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (See Fig. 4)	V_{DGO}	max.	40	V
Gate-source voltage (See Fig. 4)	$-V_{GSO}$	max.	40	V
Forward gate current	I_{GF}	max.	50	mA
Total power dissipation up to $T_{amb} = 65\ ^{o}C$	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}		-55 to $+175$	^{o}C
Junction temperature	T_j	max.	175	^{o}C

THERMAL CHARACTERISTICS*

$T_j = P\ (R_{th\ j\text{-}t} + R_{th\ t\text{-}s} + R_{th\ s\text{-}a}) + T_{amb}$

Thermal resistance

From junction to tab	$R_{th\ j\text{-}t}$	=	60	K/W
From tab to soldering points	$R_{th\ t\text{-}s}$	=	280	K/W
From soldering points to ambient**	$R_{th\ s\text{-}a}$	=	90	K/W

CHARACTERISTICS

$T_{amb} = 25\ ^{o}C$ unless otherwise specified

Gate-source cut-off current				
$V_{DS} = 0\ V; -V_{GS} = 20\ V$	$-I_{GSS}$	$<$	1	nA
Drain cut-off current				
$V_{DS} = 15\ V; -V_{GS} = 10\ V$	I_{DSX}	$<$	1	nA

			BSR56	BSR57	BSR58	
Drain current ▲						
$V_{DS} = 15\ V; V_{GS} = 0$	I_{DSS}	$>$	50	20	8	mA
		$<$	–	100	80	mA
Gate-source breakdown voltage						
$-I_G = 1\ \mu A; V_{DS} = 0$	$-V_{(BR)GSS}$	$>$	40	40	40	V
Gate-source cut-off voltage						
$I_D = 0,5\ nA; V_{DS} = 15\ V$	$-V_{(P)GS}$	$>$	4	2	0,8	V
		$<$	10	6	4	V
Drain-source voltage (on)						
$I_D = 20\ mA; V_{GS} = 0$	V_{DSon}	$<$	750	–	–	mV
$I_D = 10\ mA; V_{GS} = 0$	V_{DSon}	$<$	–	500	–	mV
$I_D = 5\ mA; V_{GS} = 0$	V_{DSon}	$<$	–	–	400	mV
Drain-source resistance (on) at f = 1 kHz						
$I_D = 0; V_{GS} = 0$	$r_{ds\ on}$	$<$	25	40	60	Ω

* See *Thermal characteristics.*

** Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

▲ Measured under pulsed conditions; $t_p = 100$ ms; $\delta \leqslant 0,1$.

	BSR56	BSR57	BSR58	
Switching times*				
$V_{DD} = 10$ V; $V_{GS} = 0$				
Conditions I_D and $-V_{GSM}$				
$I_D =$	20	10	5	mA
$-V_{GSM} =$	10	6	4	V
Delay time $t_d <$	6	6	10	ns
Rise time $t_r <$	3	4	10	ns
Turn-off time $t_{off} <$	25	50	100	ns
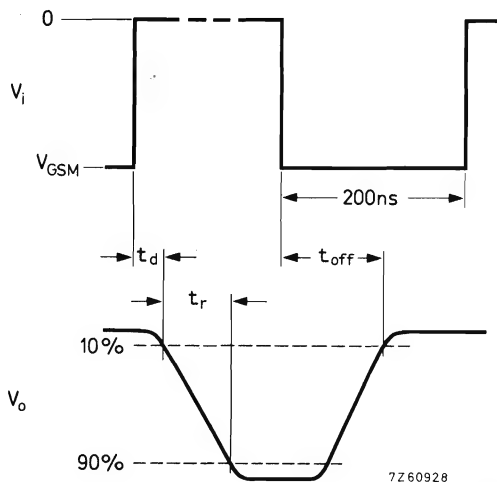
Fig. 2 Switching times waveforms.
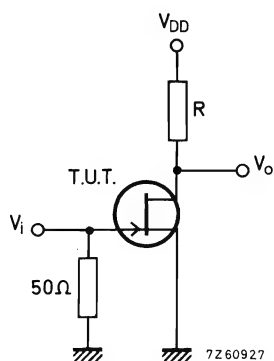
Fig. 3 Test circuit.

BSR56; R = 464 Ω
BSR57; R = 953 Ω
BSR58; R = 1910 Ω

Pulse generator

$t_r = t_f \leqslant 1$ ns
δ = 0,02
Z_o = 50 Ω

Oscilloscope

$t_r \leqslant 0,75$ ns
$R_i \geqslant$ 1 MΩ
$C_i \leqslant$ 2,5 pF

* Switching times measured on devices in SOT-18 envelope.

7Z82736

Fig. 4 Voltage derating curve.

7Z82724
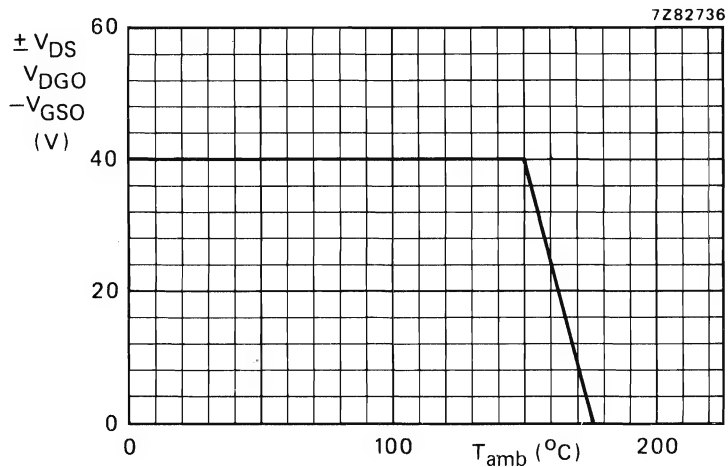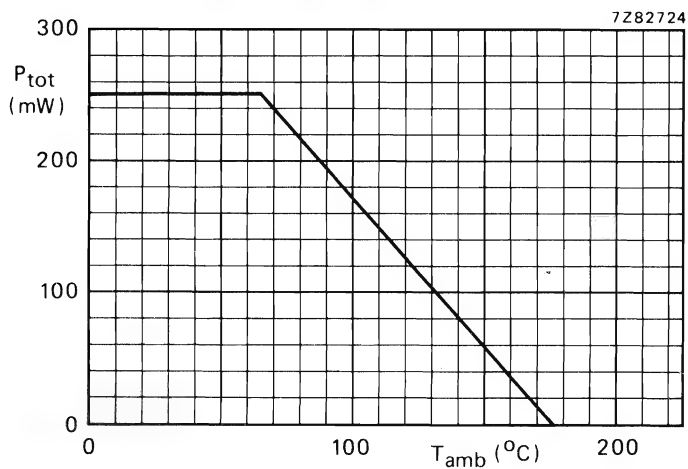
Fig. 5 Power derating curve.

DEVELOPMENT DATA
This data sheet contains advance information and
specifications are subject to change without notice.

BSR174 to 177

P-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Silicon symmetrical p-channel junction FETs in plastic microminiature SOT-23 envelopes and containing a BSJ174, 175, 176 or 177 crystal.

They are intended for application with analogue switches, choppers, commutators etc. using SMD technology.

A special feature is the interchangeability of the drain and source connections.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30		V
Gate-source voltage	V_{GSO}	max.	30		V
Gate current	$-I_G$	max.	50		mA
Total power dissipation up to $T_{amb} = 25\,^{\circ}C$	P_{tot}	max.	300		mW

			BSR174	BSR175	BSR176	BSR177	
Drain current $-V_{DS} = 15$ V; $V_{GS} = 0$	$-I_{DSS}$	>	20	7	2	1,5	mA
		<	135	70	35	20	mA
Drain-source ON-resistance $-V_{DS} = 0,1$ V; $V_{GS} = 0$	$R_{DS\,on}$	<	85	125	250	300	Ω

MECHANICAL DATA

Fig. 1 SOT-23.

Pinning:
1 = Drain
2 = Source
3 = Gate
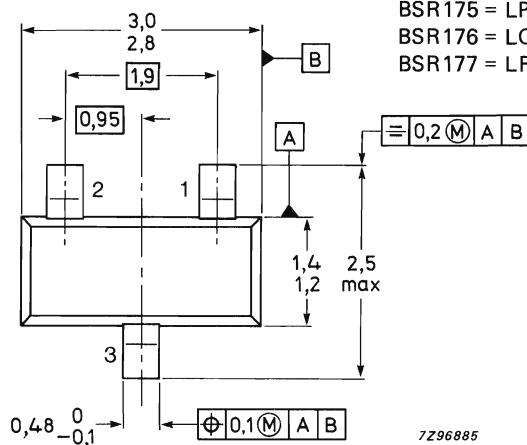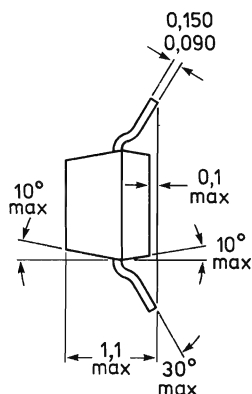
Dimensions in mm

Marking codes:
BSR174 = LO
BSR175 = LP
BSR176 = LQ
BSR177 = LR

TOP VIEW

7Z96885

Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	V_{GSO}	max.	30	V
Gate-drain voltage	V_{GDO}	max.	30	V
Gate current (d.c.)	$-I_G$	max.	50	mA
Total power dissipation up to $T_{amb} = 25\ ^oC^*$	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}		-65 to $+150$	^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\,j\text{-}a}$	=	430	K/W

STATIC CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

			BSR174	BSR175	BSR176	BSR177	
Gate cut-off current $-V_{GS} = 20$ V; $V_{DS} = 0$	I_{GSS}	<	1	1	1	1	nA
Drain cut-off current $-V_{DS} = 15$ V; $-V_{GS} = 10$ V	$-I_{DSX}$	<	1	1	1	1	nA
Drain current $-V_{DS} = 15$ V; $V_{GS} = 0$	$-I_{DSS}$	>	20	7	2	1,5	mA
		<	135	70	35	20	mA
Gate-source breakdown voltage $I_G = 1\ \mu A$; $V_{DS} = 0$	$V_{(BR)GSS}$	>	30	30	30	30	V
Gate-source cut-off voltage $-I_D = 10$ nA; $V_{DS} = 0$	$V_{GS\,off}$	>	5	3	1	0,8	V
		<	10	6	4	2,25	V
Drain-source ON-resistance $-V_{DS} = 0,1$ V; $V_{GS} = 0$	$R_{DS\,on}$	<	85	125	250	300	Ω

* Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

DEVELOPMENT DATA

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Input capacitance, f = 1 MHz

$-V_{GS}$ = 10 V; V_{DS} = 0 V	C_{is}	typ.	8	pF
$-V_{GS}$ = V_{DS} = 0	C_{is}	typ.	30	pF

Feedback capacitance, f = 1 MHz

$-V_{GS}$ = 10 V; V_{DS} = 0 V	C_{rs}	typ.	4	pF

Switching times (see Fig. 2 + 3)

			BSR174	BSR175	BSR176	BSR177	
Delay time	t_d	typ.	2	5	15	20	ns
Rise time	t_r	typ.	5	10	20	25	ns
Turn-on time	t_{on}	typ.	7	15	35	45	ns
Storage temperature	t_s	typ.	5	10	15	20	ns
Fall time	t_f	typ.	10	20	20	25	ns
Turn-off time	t_{off}	typ.	15	30	35	45	ns

Test conditions:

$-V_{DD}$	10	6	6	6	V
$V_{GS\,off}$	12	8	6	3	V
R_L	560	1200	2000	2900	Ω
$V_{GS\,on}$	0	0	0	0	V

Rise time input voltage $<$ 1 ns

Fig. 2 Switching times test circuit

Fig. 3 Input and output waveforms

$t_d + t_r = t_{on}$

$t_s + t_f = t_{off}$

N-CHANNEL FETS

Silicon symmetrical n-channel junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for switching applications. The devices have the feature: low 'on' resistance at zero gate voltage.

QUICK REFERENCE DATA

			BSV78	BSV79	BSV80	
Drain-source voltage	$\pm V_{DS}$	max.		40		V
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.		350		mW
Drain current $V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}	$>$	50	20	10	mA
Gate-source cut-off voltage $I_D = 1$ nA; $V_{GS} = 15$ V	$-V_{(P)GS}$	$>$ $<$	3,75 11	2,0 7,0	1,0 5,0	V V
Drain-source resistance (on) at f = 1 kHz $I_D = 0$; $V_{GS} = 0$	$r_{ds\ on}$	$<$	25	40	60	Ω
Feedback capacitance at f = 1 MHz $V_{DS} = 0$; $-V_{GS} = 10$ V	C_{rs}	$<$	5	5	5	pF
Turn-on time	t_{on}	$<$	10	18	30	ns
Turn-off time	t_{off}	$<$	10	16	32	ns

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-18.

Gate connected to case

Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	40	V
Forward gate current	I_G	max.	50	mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	350	mW
Storage temperature	T_{stg}	-65 to $+200$		^oC
Operating junction temperature	T_j	max.	175	^oC

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Gate cut-off currents

$-V_{GS} = 20$ V; $V_{DS} = 0$	$-I_{GSS}$	<	0.25	nA
$-V_{GS} = 20$ V; $V_{DS} = 0$; $T_j = 150\ ^oC$	$-I_{GSS}$	<	0.5	μA

Drain cut-off current

$V_{DS} = 15$ V; $-V_{GS} = 12$ V	I_{DSX}	<	0.25	nA
$V_{DS} = 15$ V; $-V_{GS} = 12$ V; $T_j = 150\ ^oC$	I_{DSX}	<	0.5	μA

			BSV78	BSV79	BSV80	
Drain current						
$V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}	>	50	20	10	mA
Gate-source cut-off voltage						
$I_D = 1$ nA; $V_{DS} = 15$ V	$-V_{(P)GS}$	>	3.75	2.0	1.0	V
		<	11	7.0	5.0	V
Gate-source voltage						
$I_D = 1.5\ \mu$A; $V_{DS} = 15$ V	$-V_{GS}$	>	3.5	1.75	0.75	V
		<	10	6.0	4.0	V
Drain-source voltage (on)						
$I_D = 20$ mA; $V_{GS} = 0$	V_{DSon}	<	500			mV
$I_D = 10$ mA; $V_{GS} = 0$	V_{DSon}	<		400		mV
$I_D = 5$ mA; $V_{GS} = 0$	V_{DSon}	<	--		325	mV
Drain-source resistance (on) at f = 1 kHz						
$I_D = 0$; $V_{GS} = 0$	$r_{ds\,on}$	<	25	40	60	Ω
y parameters at f = 1 MHz (common source)						
$-V_{GS} = 10$ V; $V_{DS} = 0$						
Input capacitance	C_{is}	<	10	10	10	pF
Feedback capacitance	$-C_{rs}$	<	5	5	5	pF

Switching times (see Fig. 2)

Turn-on time when switched from

$-V_{GSMoff} = 11$ V to $I_{Don} = 20$ mA; $V_{DD} = 10$ V **(BSV78)**
$-V_{GSMoff} = 7$ V to $I_{Don} = 10$ mA; $V_{DD} = 10$ V **(BSV79)**
$-V_{GSMoff} = 5$ V to $I_{Don} = 5$ mA; $V_{DD} = 10$ V **(BSV80)**

			BSV78	BSV79	BSV80	
delay time	t_d	<	5	10	10	ns
rise time	t_r	<	5	8	20	ns
turn-on time	t_{on}	<	10	18	30	ns

Turn-off time when switched from

$I_{Don} = 20$ mA to $-V_{GSMoff} = 11$ V; $V_{DD} = 10$ V **(BSV78)**
$I_{Don} = 10$ mA to $-V_{GSMoff} = 7$ V; $V_{DD} = 10$ V **(BSV79)**
$I_{Don} = 5$ mA to $-V_{GSMoff} = 5$ V; $V_{DD} = 10$ V **(BSV80)**

fall time	t_f	<	6	11	24	ns
storage time	t_s	<	4	5	8	ns
turn-off time	t_{off}	<	10	16	32	ns
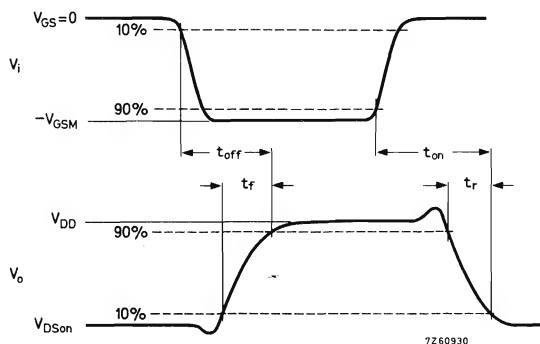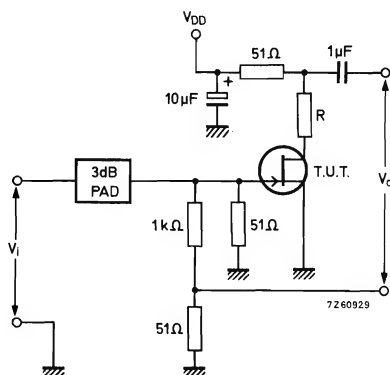
Fig. 2 Switching times test circuit and input and output waveforms.

$$R = \frac{10 - V_{DSon}\ (V)}{I_{Don}\ (A)} - 51$$

	BSV78	BSV79	BSV80	
R =	424	909	1885	Ω

Pulse generator:

$R_i = 50\ \Omega$
$t_r < 0{,}5$ ns
$t_f < 5$ ns

Oscilloscope:

$R_i = 50\ \Omega$
$t_r < 1$ ns
$t_f < 1$ ns

typical values
$T_j = 25°C$
$V_{DS} = 1V$

BSV 78
BSV 79
BSV 80

7Z60758

BSV78

typical characteristics
under pulse conditions
$T_j = 25°C$

I_D (mA)

$V_{GS} = 0V$
-0.5V
-1V
-1.5V
-2V
-2.5V
-3V
-3.5V
-4V
-4.5V
-5V

$V_{DS} = 15V$

V_{GS} (V)

V_{DS} (V)

7Z60760

BSV79

typical characteristics
under pulse conditions
$T_j = 25°C$

I_D (mA)

$V_{GS} = 0V$
-0.5V
-1V
-1.5V
-2V
-2.5V
-3V
-3.5V
-4V

$V_{DS} = 15V$

V_{GS} (V)

V_{DS} (V)

correlation band between $r_{ds\,on}$ and I_{DSS}

$r_{ds\,on}$ (Ω)

$I_D = 0$
$V_{DS} = 0$
$f = 1\,kHz$
$T_j = 25°C$

7Z61183

I_{DSS} at $V_{DS} = 15V$ (mA)

correlation band between $-V_{GS}$ and I_{DSS}

$-V_{GS}$ (V)

$I_D = 1.5\,\mu A$
$V_{DS} = 15\,V$
$T_j = 25°C$

7Z61184

I_{DSS} at $V_{DS} = 15V$ (mA)

N-CHANNEL FETS

Symmetrical silicon n-channel depletion type junction field-effect transistors on a plastic microminiature envelope intended for application in thick and thin-film circuits. The transistors are intended for low-power chopper or switching applications in industry.

QUICK REFERENCE DATA

			PMBF4391	PMBF4392	PMBF4393	
Drain-source voltage	$\pm V_{DS}$	max.	40	40	40	V
Drain current $V_{DS} = 20$ V; $V_{GS} = 0$	I_{DSS}	>	50	25	5	mA
Gate-source cut-off voltage $V_{DS} = 20$ V; $I_D = 1$ nA	$-V_{(P)GS}$	> <	4 10	2 5	0,5 3	V V
Drain-source resistance (on) at f = 1 kHz $I_D = 1$ mA; $V_{GS} = 0$	$r_{ds\,on}$	<	30	60	100	Ω
Feedback capacitance at f = 1 MHz $-V_{GS} = 12$ V; $V_{DS} = 0$	C_{rs}	<	3,5	3,5	3,5	pF
Turn-off time $V_{DD} = 10$ V; $V_{GS} = 0$						
$I_D = 12$ mA; $-V_{GSM} = 12$ V	t_{off}	<	20	—	—	ns
$I_D = 6$ mA; $-V_{GSM} = 7$ V	t_{off}	<	—	35	—	ns
$I_D = 3$ mA; $-V_{GSM} = 5$ V	t_{off}	<	—	—	50	ns

MECHANICAL DATA

Fig. 1 SOT-23.

Dimensions in mm

Marking code
PMBF4391 = M62
PMBF4392 = M63
PMBF4393 = M64

TOP VIEW

Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage (See Fig. 4)	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (See Fig. 4)	V_{DGO}	max.	40	V
Gate-source voltage (See Fig. 4)	$-V_{GSO}$	max.	40	V
Gate current (d.c.)	I_G	max.	50	mA
Total power dissipation up to $T_{amb} = 65\ ^oC$	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}		-65 to $+175$	^oC
Junction temperature	T_j	max.	175	^oC

THERMAL CHARACTERISTICS

$T_j = P (R_{th\ j\text{-}t} + R_{th\ t\text{-}s} + R_{th\ s\text{-}a}) + T_{amb}$

Thermal resistance

From junction to tab	$R_{th\ j\text{-}t}$	=	60	K/W
From tab to soldering points	$R_{th\ t\text{-}s}$	=	260	K/W
From soldering points to ambient *	$R_{th\ s\text{-}a}$	=	120	K/W

CHARACTERISTICS

$T_{amb} = 25\ ^oC$ unless otherwise specified

Gate-source voltage				
$I_G = 1$ mA; $V_{DS} = 0$	V_{GSon}	<	1	V
Gate-source cut-off current				
$V_{DS} = 0$ V; $-V_{GS} = 20$ V	$-I_{GSS}$	<	1	nA
$V_{DS} = 0$ V; $-V_{GS} = 20$ V; $T_{amb} = 150\ ^oC$	$-I_{GSS}$	<	0,2	μA

			PMBF4391	PMBF4392	PMBF4393	
Drain current**						
$V_{DS} = 20$ V; $V_{GS} = 0$	I_{DSS}	>	50	25	5	mA
		<	150	75	30	mA
Gate-source breakdown voltage						
$-I_G = 1\ \mu A$; $V_{DS} = 0$	$-V_{(BR)GSS}$	>	40	40	40	V
Gate-source cut-off voltage						
$I_D = 1$ nA; $V_{DS} = 20$ V	$-V_{(P)GS}$	>	4	2	0,5	V
		<	10	5	3	V
Drain-source voltage (on)						
$I_D = 12$ mA; $V_{GS} = 0$	V_{DSon}	<	0,4	–	–	V
$I_D = 6$ mA; $V_{GS} = 0$	V_{DSon}	<		0,4	–	V
$I_D = 3$ mA; $V_{GS} = 0$	V_{DSon}	<	–	–	0,4	V
Drain-source resistance (on)						
$I_D = 0$; $V_{GS} = 0$; $f = 1$ kHz	$r_{ds\ on}$	<	30	60	100	Ω

   → * Mounted on a ceramic substrate of 7 mm x 5 mm x 0,7 mm.
     ** Measured under pulsed conditions; $t_p = 100\ \mu s$; $\delta = 0,01$.

			PMBF4391	PMBF4392	PMBF4393	
Drain cut-off current						
$-V_{GS}$ = 12 V	I_{DSX}	<	1	–	–	nA
$-V_{GS}$ = 7 V $\rbrace V_{DS}$ = 20 V	I_{DSX}	<	–	1	–	nA
$-V_{GS}$ = 5 V	I_{DSX}	<	–	–	1	nA
$-V_{GS}$ = 12 V	I_{DSX}	<	0,2	–	–	μA
$-V_{GS}$ = 7 V $\rbrace V_{DS}$ = 20 V; T_{amb} = 150 °C	I_{DSX}	<	–	0,2	–	μA
$-V_{GS}$ = 5 V	I_{DSX}	<	–	–	0,2	μA

y-parameters (common source)
V_{DS} = 20 V; V_{GS} = 0; f = 1 MHz

			PMBF4391	PMBF4392	PMBF4393	
Input capacitance	C_{is}	<	14	14	14	pF
Feedback capacitance	C_{rs}	<	3,5	3,5	3,5	pF

Switching times
V_{DD} = 10 V; V_{GS} = 0
Conditions I_D and $-V_{GSM}$

			PMBF4391	PMBF4392	PMBF4393	
	I_D	=	12	6	3	mA
	$-V_{GSM}$	=	12	7	5	V
Rise time	t_r	<	5	5	5	ns
Turn on time	t_{on}	<	15	15	15	ns
Fall time	t_f	<	15	20	30	ns
Turn off time	t_{off}	<	20	35	50	ns

Fig. 2 Switching times waveforms.
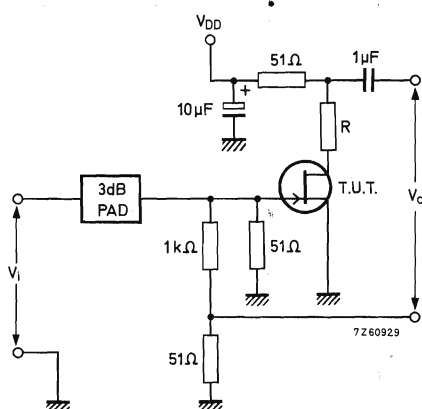
$$R = \frac{9,6}{I_D} - 51\ \Omega$$

Pulse generator:

t_r	$<$	0,5 ns
t_f	$<$	0,5 ns
t_p	$=$	100 μs
δ	$=$	0,01

Oscilloscope:

R_i $=$ 50 Ω

Fig. 3 Test circuit.
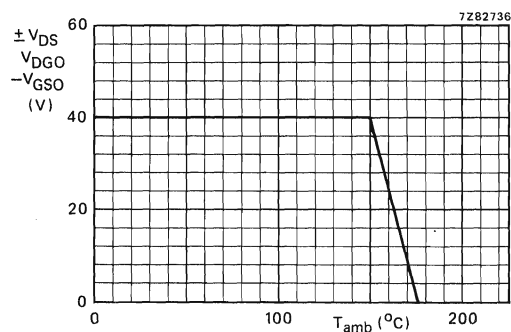
Fig. 4 Voltage derating curve.
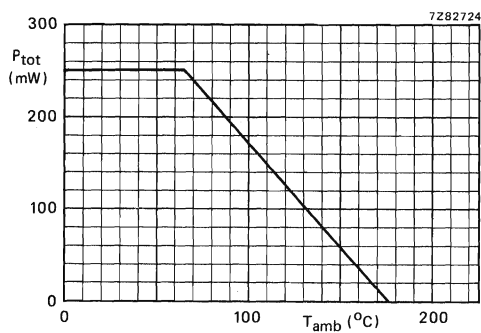
Fig. 5 Power derating curve.

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR

Symmetrical n-channel, depletion type, silicon junction field-effect transistor, designed primarily for small-signal general purpose high-frequency amplifier applications. The 2N3822 features low gate leakage current and low input capacitance.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	50 V
Gate-source voltage	$-V_{GS}$	max.	50 V
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	300 mW
Drain current $V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}		2 to 10 mA
Transfer admittance (common source) $V_{DS} = 15$ V; $V_{GS} = 0$; f = 1 kHz	$\lvert Y_{fs} \rvert$		3,0 to 6,5 mS
$V_{DS} = 15$ V; $V_{GS} = 0$; f = 100 MHz	$\lvert Y_{fs} \rvert$	$>$	3,0 mS

MECHANICAL DATA   Dimensions in mm
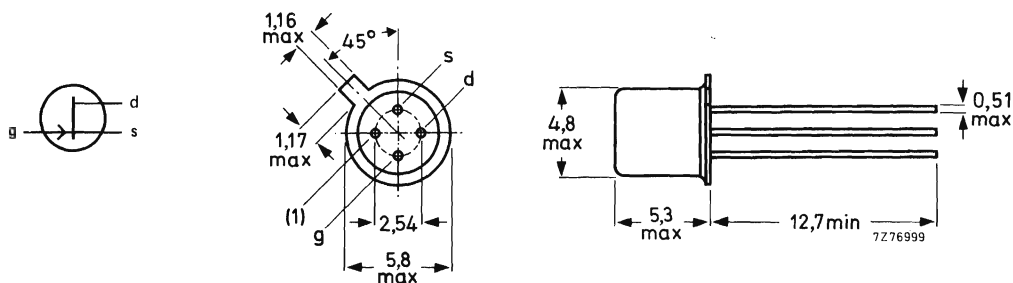
Fig. 1 TO-72.

Note: Drain and source are interchangeable.

(1) Shield lead connected to case.

Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	50	V
Drain-gate voltage	V_{DG}	max.	50	V
Gate-source voltage	$-V_{GS}$	max.	50	V
Gate current (d.c.)	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Storage temperature	T_{stg}		-65 to $+200$	°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	$\approx$	590	K/W

CHARACTERISTICS with source connected to case for all measurements

T_{amb} = 25 °C unless otherwise specified

Gate cut-off current				
$-V_{GS}$ = 30 V; V_{DS} = 0	$-I_{GSS}$	$<$	0,1	nA
$-V_{GS}$ = 30 V; V_{DS} = 0; T_{amb} = 150 °C	$-I_{GSS}$	$<$	0,1	μA
Drain current *				
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		2 to 10	mA
Gate-source breakdown voltage				
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	$>$	50	V
Gate-source voltage				
V_{DS} = 15 V; I_D = 200 μA	$-V_{GS}$		1 to 4	V
Gate-source cut-off voltage				
V_{DS} = 15 V; I_D = 0,5 nA	$-V_{(P)GS}$	$<$	6	V

Small-signal common source characteristics

V_{DS} = 15 V; V_{GS} = 0

Transfer admittance *				
f = 1 kHz	$|y_{fs}|$		3,0 to 6,5	mS
f = 100 MHz	$|y_{fs}|$	$>$	3,0	mS
Output admittance at f = 1 kHz *	$|y_{os}|$	$<$	20	μS
Input capacitance at f = 1 MHz	C_{is}	$<$	6	pF
Feedback capacitance at f = 1 MHz	C_{rs}	$<$	3	pF
Noise figure				
V_{DS} = 15 V; V_{GS} = 0; R_G = 1 MΩ				
f = 10 Hz; B = 5 Hz	F	$<$	5	dB
Equivalent input noise voltage				
V_{DS} = 15 V; V_{GS} = 0				
f = 10 Hz; B = 5 Hz	V_n	$<$	200	nV/$\sqrt{\text{Hz}}$

* Measured under pulse conditions: t_p = 100 ms; $\delta \leqslant 0,1$.

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR

Symmetrical n-channel, depletion type, silicon planar epitaxial junction field-effect transistor in a TO-72 metal envelope, intended for v.h.f. amplifier and mixer applications in industrial service.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	$-V_{GS}$	max.	30	V
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	300	mW
Drain current $V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}		4 to 20	mA
Feedback capacitance at f = 1 MHz $V_{DS} = 15$ V; $V_{GS} = 0$	C_{rs}	$<$	2	pF
Transfer admittance (common source) $V_{DS} = 15$ V; $V_{GS} = 0$; f = 200 MHz	$\lvert y_{fs} \rvert$	$>$	3,2	mS
Noise figure at f = 100 MHz $V_{DS} = 15$ V; $V_{GS} = 0$; $R_G = 1$ kΩ	F	$<$	2,5	dB

MECHANICAL DATA
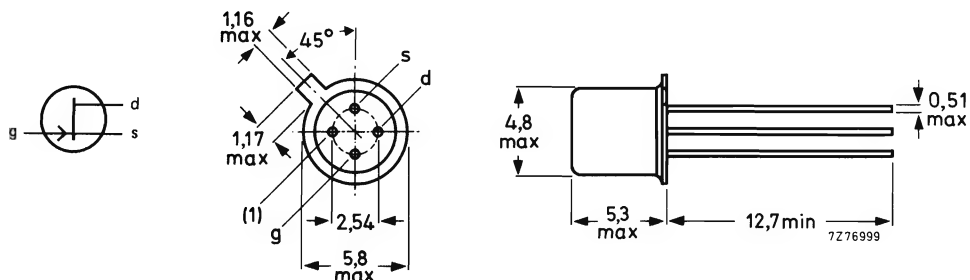
Dimensions in mm

Fig. 1 TO-72.

Note: Drain and source are interchangeable.

(1) Shield lead connected to case.

Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage	V_{DG}	max.	30 V
Gate-source voltage	$-V_{GS}$	max.	30 V
Gate current (d.c.)	I_G	max.	10 mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	300 mW
Storage temperature	T_{stg}		-65 to $+200\ ^oC$
Junction temperature	T_j	max.	200 ^oC

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	590 K/W

CHARACTERISTICS with source and shield connected to case for all measurements

$T_{amb} = 25\ ^oC$ unless otherwise specified

Gate cut-off current			
$-V_{GS} = 20$ V; $V_{DS} = 0$	$-I_{GSS}$	<	0,5 nA
$-V_{GS} = 20$ V; $V_{DS} = 0$; $T_{amb} = 150\ ^oC$	$-I_{GSS}$	<	0,5 μA
Drain current *			
$V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}		4 to 20 mA
Gate-source breakdown voltage			
$-I_G = 1\ \mu A$; $V_{DS} = 0$	$-V_{(BR)GSS}$	>	30 V
Gate-source voltage			
$I_D = 400\ \mu A$; $V_{DS} = 15$ V	$-V_{GS}$		1,0 to 7,5 V
Gate-source cut-off voltage			
$V_{DS} = 15$ V; $I_D = 0,5$ nA	$-V_{(P)GS}$	<	8 V

Small-signal common source characteristics

$V_{DS} = 15$ V; $V_{GS} = 0$

Transfer admittance *			
$f = 1$ kHz	$\|y_{fs}\|$		3,5 to 6,5 mS
$f = 200$ MHz	$\|y_{fs}\|$	>	3,2 mS
Output admittance at $f = 1$ kHz *	$\|y_{os}\|$	<	35 μS
Input capacitance at $f = 1$ MHz	C_{is}	<	6 pF
Feedback capacitance at $f = 1$ MHz	C_{rs}	<	2 pF
Real part of input conductance at $f = 200$ MHz	$Re(y_{is})$	<	0,8 mS
Real part of output conductance at $f = 200$ MHz	$Re(y_{os})$	<	0,2 mS
Noise figure at $f = 100$ MHz			
$V_{DS} = 15$ V; $V_{GS} = 0$; $R_G = 1$ kΩ	F	<	2,5 dB

* Measured under pulse conditions: $t_p = 100$ ms; $\delta \leqslant 0,1$.

N-CHANNEL SILICON FET

Symmetrical n-channel planar epitaxial junction field-effect transistor in a TO-72 metal envelope with the shield lead connected to the case. The transistor is suitable in a variety of low power switching applications, e.g. in multiplexing systems.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Total power dissipation up to $T_{amb} = 25\ ^{o}C$	P_{tot}	max.	300	mW
Drain current $V_{DS} = 20$ V; $V_{GS} = 0$	I_{DSS}	>	2	mA
Gate-source cut-off voltage $I_D = 10$ nA; $V_{DS} = 10$ V	$-V_{(P)GS}$		4 to 6	V
Feedback capacitance at f = 1 MHz $V_{DS} = 0$; $V_{GS} = 7$ V	C_{rs}	<	1,5	pF
Drain-source resistance (on) at f = 1 kHz $V_{GS} = 0$; $I_D = 0$	$R_{DS(on)}$	<	220	Ω

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.

(1) = shield lead connected to case

Accessories: 56246 (distance disc).

Note: Drain and source are interchangeable

RATINGS   Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Gate current	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 25 $^{\circ}$C	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}	-55 to $+200$		$^{\circ}$C
Junction temperature	T_j	max.	200	$^{\circ}$C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	**590**	K/W

CHARACTERISTICS $T_j = 25\ ^{\circ}C$ unless otherwise specified

Gate cut-off currents

$-V_{GS} = 20\ V; V_{DS} = 0$ $\quad -I_{GSS}$ $\quad <$ $\quad 0.1$ $\quad nA$

Drain current

$V_{DG} = 20\ V; I_S = 0$ $\quad I_{DGO}$ $\quad <$ $\quad 0.1$ $\quad nA$

$V_{DG} = 20\ V; I_S = 0; T_{amb} = 150\ ^{\circ}C$ $\quad I_{DGO}$ $\quad <$ $\quad 0.2$ $\quad \mu A$

Drain current [1])

$V_{DS} = 20\ V; V_{GS} = 0$ $\quad I_{DSS}$ $\quad >$ $\quad 2$ $\quad mA$

Gate-source breakdown voltage

$-I_G = 1.0\ \mu A; V_{DS} = 0$ $\quad -V_{(BR)GS}$ $\quad >$ $\quad 30$ $\quad V$

Gate-source voltage

$I_D = 10\ nA; V_{DS} = 10\ V$ $\quad -V_{(P)GS}$ $\quad 4\ to\ 6$ $\quad V$

Drain-source voltage

$I_D = 1.0\ mA; V_{GS} = 0$ $\quad V_{DS}$ $\quad <$ $\quad 0.25$ $\quad V$

Drain cut-off current

$V_{DS} = 10\ V; -V_{GS} = 7.0\ V$ $\quad I_D$ $\quad <$ $\quad 1.0$ $\quad nA$

$V_{DS} = 10\ V; -V_{GS} = 7.0\ V; T_{amb} = 150\ ^{\circ}C$ $\quad I_D$ $\quad <$ $\quad 2.0$ $\quad \mu A$

Drain-source resistance (on) at f = 1 kHz

$V_{GS} = 0; I_D = 0$ $\quad R_{DS(on)}$ $\quad <$ $\quad 220$ $\quad \Omega$

Input capacitance at f = 1 MHz

$V_{DS} = 20\ V; V_{GS} = 0$ $\quad C_{is}$ $\quad <$ $\quad 6$ $\quad pF$

Feedback capacitance at f = 1 MHz

$V_{DS} = 0; V_{GS} = 7\ V$ $\quad -C_{rs}$ $\quad <$ $\quad 1.5$ $\quad pF$

Switching times

$V_{DD} = 1.5\ V; I_{D\ on} = 1.0\ mA$

$V_{GS\ on} = 0; -V_{GS\ off} = 6\ V$

delay time	t_d	<	20	ns
rise time	t_r	<	100	ns
turn off time	t_{off}	<	100	ns

CHARACTERISTICS (continued)

Switching times

$V_{DD} = 1.5$ V; $I_{D\,on} = 1.0$ mA

$V_{GS\,on} = 0$; $-V_{GS\,off} = 6$ V

delay time	t_d	<	20	ns
rise time	t_r	<	100	ns
turn off time	t_{off}	<	100	ns
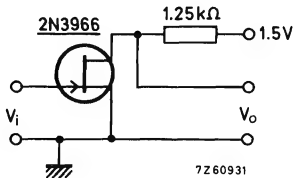
Fig. 2 Test circuit
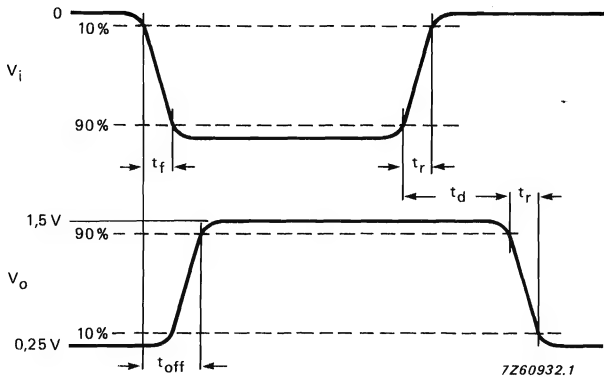
Fig. 3 Waveforms

Pulse generator:

t_r < 1.0 ns
t_f < 1.0 ns
t_p = 1.0 μs
δ < 0.5
R_S = 50 Ω

Oscilloscope:

t_r < 10 ns
R_i > 5 MΩ
C_i < 10 pF

N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power switching applications in industrial service.

QUICK REFERENCE DATA

			2N4091	2N4092	2N4093	
Drain-source voltage	$\pm V_{DS}$	max.		40		V
Total power dissipation up to $T_{case} = 25\ ^{o}C$	P_{tot}	max		1,8		W
Drain current $V_{DS} = 20$ V; $V_{GS} = 0$	I_{DSS}	>	30	15	8	mA
Gate-source cut-off voltage $I_D = 1$ nA; $V_{DS} = 20$ V	$-V_{(P)GS}$	> <	5,0 10	2,0 7,0	1,0 5,0	V V
Drain-source resistance (on) at f = 1 kHz $I_D = 0$; $V_{GS} = 0$	$r_{ds\ on}$	<	30	50	80	Ω
Feedback capacitance at f = 1 MHz $V_{DS} = 0$; $-V_{GS} = 20$ V	C_{rs}	<		5,0		pF
Turn-off time $V_{DD} = 3,0$ V; $V_{GS} = 0$						
$I_D = 6,6$ mA; $-V_{GSM} = 12$ V 2N4091	t_{off}	<		40		ns
$I_D = 4,0$ mA; $-V_{GSM} = $ 8 V 2N4092	t_{off}	<		60		ns
$I_D = 2,5$ mA; $-V_{GSM} = $ 6 V 2N4093	t_{off}	<		80		ns

MECHANICAL DATA
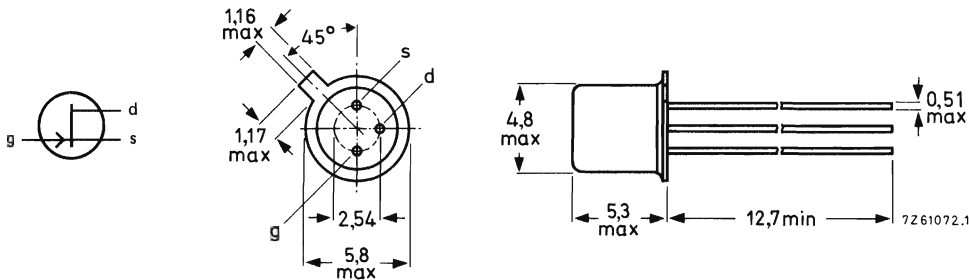
Dimensions in mm

Fig. 1 TO-18.

Gate connected to case

Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	40	V

Current

Forward gate current (d.c.)	I_G	max.	10	mA

Total power dissipation up to $T_{case} = 25\ ^oC$	P_{tot}	max.	1.8	W

Storage temperature	T_{stg}	-55 to $+200$		^oC
Junction temperature	T_j	max.	200	^oC

THERMAL RESISTANCE

From junction to case in free air	$R_{th\ j-c}$	=	100	K/W

CHARACTERISTICS

T_{amb} = 25 ^{o}C unless otherwise specified

Drain currents

			2N4091	2N4092	2N4093	
V_{DG} = 20 V; I_S = 0	I_{DGO}	<		0.2		nA
V_{DG} = 20 V; I_S = 0; T_{amb} = 150 ^{o}C	I_{DGO}	<		0.4		µA

Source current

V_{SG} = 20 V; I_D = 0	I_{SGO}	<		0.2		nA

Drain cut-off current

			2N4091	2N4092	2N4093	
V_{DS} = 20 V; $-V_{GS}$ = 12 V	I_{DSX}	<	0.2	–	–	nA
V_{DS} = 20 V; $-V_{GS}$ = 8 V	I_{DSX}	<	–	0.2	–	nA
V_{DS} = 20 V; $-V_{GS}$ = 6 V	I_{DSX}	<	–	–	0.2	nA
V_{DS} = 20 V; $-V_{GS}$ = 12 V; T_{amb} = 150 ^{o}C	I_{DSX}	<	0.4	–	–	µA
V_{DS} = 20 V; $-V_{GS}$ = 8 V; T_{amb} = 150 ^{o}C	I_{DSX}	<	–	0.4	–	µA
V_{DS} = 20 V; $-V_{GS}$ = 6 V; T_{amb} = 150 ^{o}C	I_{DSX}	<	–	–	0.4	µA

Gate-source breakdown voltage

$-I_G$ = 1.0 µA; V_{DS} = 0	$-V_{(BR)GSS}$	>	40	40	40	V

Drain current [1])

V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	30	15	8	mA

Gate-source cut-off voltage

I_D = 1 nA; V_{DS} = 20 V	$-V_{(P)GS}$	>	5.0	2.0	1.0	V
		<	10	7.0	5.0	V

Drain-source voltages (on)

I_D = 6.6 mA; V_{GS} = 0	V_{DSon}	<	0.2	–	–	V
I_D = 4.0 mA; V_{GS} = 0	V_{DSon}	<	–	0.2	–	V
I_D = 2.5 mA; V_{GS} = 0	V_{DSon}	<	–	–	0.2	V

Drain-source resistance (on)

I_D = 1.0 mA; V_{GS} = 0	r_{DSon}	<	30	50	80	Ω

Drain-source resistance (on) at f = 1 kHz

I_D = 0; V_{GS} = 0	$r_{ds\ on}$	<	30	50	80	Ω

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[1]) Measured under pulsed conditions: $t_p \leq 300$ µs; $\delta \leq 0.03$

CHARACTERISTICS (continued) $T_{amb} = 25\ ^\circ C$ unless otherwise specified

y-parameters at f = 1 MHz (common source)

Input capacitance

$V_{DS} = 20\ V$; $V_{GS} = 0$ C_{is} <   16   pF

Feedback capacitance

$V_{DS} = 0$; $-V_{GS} = 20\ V$ C_{rs} <   5   pF

Switching times

$V_{DD} = 3, 0\ V$; $V_{GS} = 0$

			2N4091	2N4092	2N4093	
	I_D	=	6, 6	4, 0	2, 5	mA
	$-V_{GSM}$	=	12	8	6	V
Delay time	t_d	<	15	15	20	ns
Rise time	t_r	<	10	20	40	ns
Turn-off time	t_{off}	<	40	60	80	ns

Test circuit:
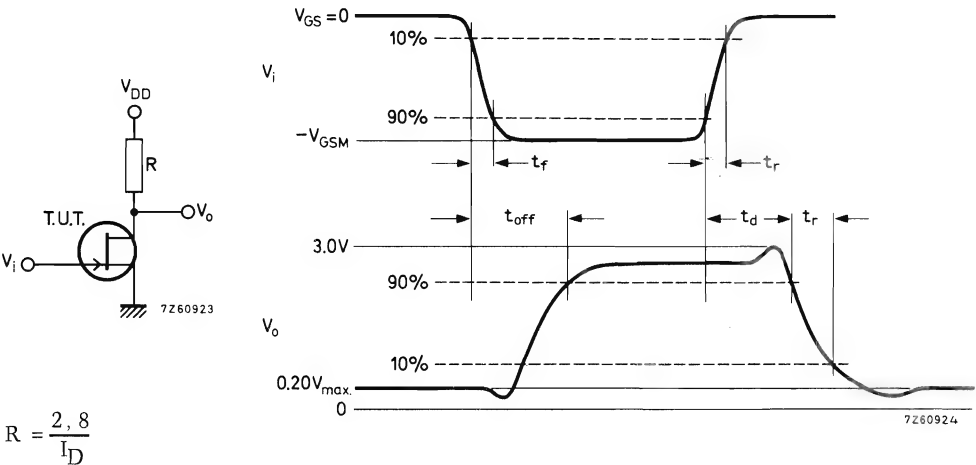
$$R = \frac{2,8}{I_D}$$

Pulse generator:

t_r	<	1	ns
t_f	<	1	ns
t_p	=	1, 0	µs
δ	=	0, 1	
R_S	=	50	Ω

Oscilloscope:

t_r	<	0, 4	ns
R_i	>	9, 8	$M\Omega$
C_i	<	1, 7	pF

N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power, chopper or switching, application in industrial service.

QUICK REFERENCE DATA

			2N4391	2N4392	2N4393	
Drain-source voltage	$\pm V_{DS}$	max.		40		V
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.		1,8		W
Drain current V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	50	25	5	mA
Gate-source cut-off voltage I_D = 1 nA; V_{DS} = 20 V	$-V_{(P)GS}$	> <	4,0 10	2,0 5,0	0,5 3,0	V V
Drain-source resistance (on) at f = 1 kHz I_D = 1 mA; V_{GS} = 0	$r_{ds\ on}$	<	30	60	100	Ω
Feedback capacitance at f = 1 MHz V_{DS} = 0; $-V_{GS}$ = 12 V 2N4391 V_{DS} = 0; $-V_{GS}$ = 7 V 2N4392 V_{DS} = 0; $-V_{GS}$ = 5 V 2N4393	C_{rs}	<	3,5	3,5	3,5	pF
Turn-off time V_{DD} = 10 V; V_{GS} = 0						
I_D = 12 mA; $-V_{GSM}$ = 12 V	t_{off}	<	20	–	–	ns
I_D = 6,0 mA; $-V_{GSM}$ = 7 V	t_{off}	<	–	35	–	ns
I_D = 3,0 mA; $-V_{GSM}$ = 5 V	t_{off}	<	–	–	50	ns
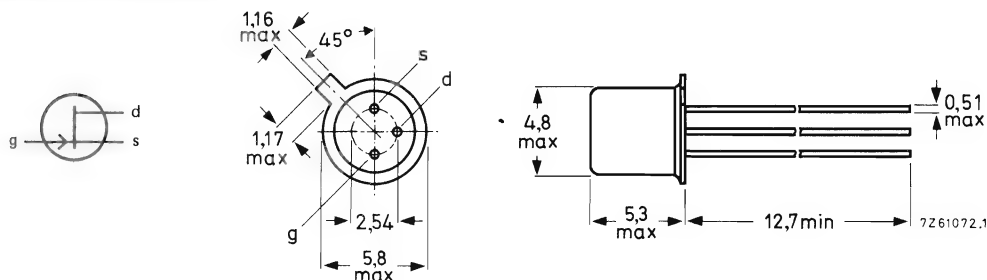
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-18.

Gate connected to case

Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V
Gate current (d.c.)	I_G	max.	50	mA
Total power dissipation up to $T_{case} = 25\,^{O}C$	P_{tot}	max.	1.8	W
Storage temperature	T_{stg}	−65 to 200		^{O}C
Junction temperature	T_j	max.	200	^{O}C
→ From junction to case in free air	$R_{th\ j-c}$	=	100	K/W

CHARACTERISTICS $T_{amb} = 25\ ^{O}C$ unless otherwise specified

Gate cut-off current

$-V_{GS} = 20$ V; $V_{DS} = 0$	$-I_{GSS} <$	0.1	nA
$-V_{GS} = 20$ V; $V_{DS} = 0$; $T_{amb} = 150\,^{O}C$	$-I_{GSS} <$	0.2	µA

Drain cut-off current

		2N4391	2N4392	2N4393	
$V_{DS} = 20$ V; $-V_{GS} = 12$ V	$I_{DSX} <$	0.1	–	–	nA
$V_{DS} = 20$ V; $-V_{GS} = 7$ V	$I_{DSX} <$	–	0.1	–	nA
$V_{DS} = 20$ V; $-V_{GS} = 5$ V	$I_{DSX} <$	–	–	0.1	nA
$V_{DS} = 20$ V; $-V_{GS} = 12$ V; $T_{amb} = 150\,^{O}C$	$I_{DSX} <$	0.2	–	–	µA
$V_{DS} = 20$ V; $-V_{GS} = 7$ V; $T_{amb} = 150\,^{O}C$	$I_{DSX} <$	–	0.2	–	µA
$V_{DS} = 20$ V; $-V_{GS} = 5$ V; $T_{amb} = 150\,^{O}C$	$I_{DSX} <$	–	–	0.2	µA

CHARACTERISTICS (continued) $T_{amb} = 25\,^{\circ}C$ unless otherwise specified

Drain currents [1]			2N4391	2N4392	2N4393	
$V_{DS} = 20$ V; $V_{GS} = 0$	I_{DSS}	>	50	–	–	mA
		<	150	–	–	mA
$V_{DS} = 20$ V; $V_{GS} = 0$	I_{DSS}	>	–	25	–	mA
		<	–	75	–	mA
$V_{DS} = 20$ V; $V_{GS} = 0$	I_{DSS}	>	–	–	5	mA
		<	–	–	30	mA
Gate-source breakdown voltage						
$-I_G = 1$ µA; $V_{DS} = 0$	$-V_{(BR)GSS}$	>	40	40	40	V
Gate-source voltage						
$I_G = 1$ mA; $V_{DS} = 0$	V_{GSon}	<	1.0	1.0	1.0	V
Gate-source cut-off voltage						
$I_D = 1$ nA; $V_{DS} = 20$ V	$-V_{(P)GS}$	>	4.0	2.0	0.5	V
		<	10	5.0	3.0	V
Drain-source voltage (on)						
$I_D = 12$ mA; $V_{GS} = 0$	V_{DSon}	<	0.4	–	–	V
$I_D = 6.0$ mA; $V_{GS} = 0$	V_{DSon}	<	–	0.4	–	V
$I_D = 3.0$ mA; $V_{GS} = 0$	V_{DSon}	<	–	–	0.4	V
Drain-source resistance (on)						
$I_D = 1$ mA; $V_{GS} = 0$	r_{DSon}	<	30	60	100	Ω
Drain-source resistance (on) at f = 1 kHz						
$I_D = 0$; $V_{GS} = 0$	r_{dson}	<	30	60	100	Ω
y parameters at f = 1 MHz (common source)						
Input capacitance						
$V_{DS} = 20$ V; $V_{GS} = 0$	C_{is}	<	14	14	14	pF
Feedback capacitance						
$-V_{GS} = 12$ V; $V_{DS} = 0$	$-C_{rs}$	<	3.5	–	–	pF
$-V_{GS} = 7$ V; $V_{DS} = 0$	$-C_{rs}$	<	–	3.5	–	pF
$-V_{GS} = 5$ V; $V_{DS} = 0$	$-C_{rs}$	<	–	–	3.5	pF

[1] measured under pulsed conditions: $t_p = 100$ µs; $\delta = 0.01$

CHARACTERISTICS (continued) T_{amb} = 25 ^{o}C unless otherwise specified

Switching times

VDD = 10 V; VGS = 0

			2N4391	2N4392	2N4393	
	I_D	=	12	6.0	3.0	mA
	$-V_{GSM}$	=	12	7	5	V
Rise time	t_r	<	5	5	5	ns
Turn on time	t_{on}	<	15	15	15	ns
Fall time	t_f	<	15	20	30	ns
Turn off time	t_{off}	<	20	35	50	ns

Test circuit:

$$R = \frac{9.6}{I_D} - 51\,\Omega$$

Pulse generator:

t_r	<	0.5	ns
t_f	<	0.5	ns
t_p	=	100	μs
δ	=	0.01	

Oscilloscope:

R_i = 50 Ω

N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power, chopper or switching, applications in industrial service.

QUICK REFERENCE DATA

				2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
Drain-source voltage	2N4856 to 2N4858	$\pm V_{DS}$	max.		40		V
	2N4859 to 2N4861	$\pm V_{DS}$	max.		30		V
Total power dissipation up to $T_{amb} = 25\,^{\circ}C$		P_{tot}	max.		360		mW
Drain current $V_{DS} = 15$ V; $V_{GS} = 0$		I_{DSS}	>	50	20	8	mA
Gate-source cut-off voltage $I_D = 0,5$ nA; $V_{DS} = 15$ V		$-V_{(P)GS}$	>	4	2	0,8	V
			<	10	6	4	V
Drain-source resistance (on) at f = 1 kHz $I_D = 0$; $V_{GS} = 0$		$r_{ds\,on}$	<	25	40	60	Ω
Feedback capacitance at f = 1 MHz $V_{DS} = 0$; $-V_{GS} = 10$ V		C_{rs}	<		8		pF
Turn-off time $V_{DD} = 10$ V; $V_{GS} = 0$							
$I_D = 20$ mA; $-V_{GSM} = 10$ V	2N4856; 2N4859	t_{off}	<		25		ns
$I_D = 10$ mA; $-V_{GSM} = 6$ V	2N4857; 2N4860	t_{off}	<		50		ns
$I_D = 5$ mA; $-V_{GSM} = 4$ V	2N4858; 2N4861	t_{off}	<		100		ns

MECHANICAL DATA
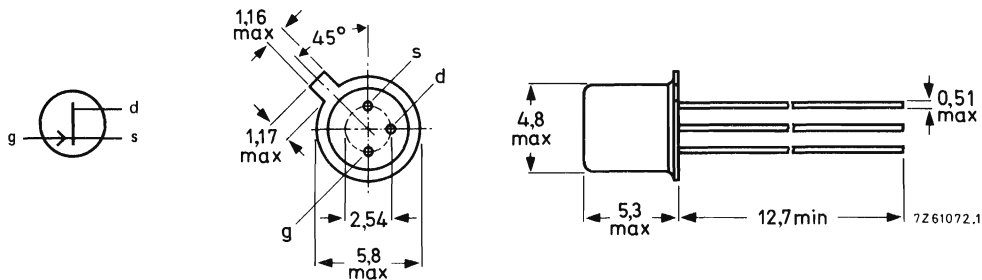
Dimensions in mm

Fig. 1 TO-18

Gate connected to case

Accessories: 56246 (distance disc).

Note: Drain and source are interchangeable.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

			2N4856 2N4857 2N4858	2N4859 2N4860 2N4861	
Drain-source voltage	$\pm V_{DS}$	max.	40	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	40	30	V
Gate current (d.c.)	I_G	max.	50		mA
Total power dissipation up to $T_{amb} = 25\,^{\circ}C$	P_{tot}	max.	360		mW
Storage temperature	T_{stg}		-65 to $+200$		$^{\circ}C$
Junction temperature	T_j	max.	200		$^{\circ}C$

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	**490**	K/W

CHARACTERISTICS

$T_{amb} = 25\,^{\circ}C$ unless otherwise specified

			2N4856 2N4857 2N4858	2N4859 2N4860 2N4861	
Gate cut-off currents					
$-V_{GS} = 20\,V;\ V_{DS} = 0$	$-I_{GSS}$	<	0.25	–	nA
$-V_{GS} = 15\,V;\ V_{DS} = 0$	$-I_{GSS}$	<	–	0.25	nA
$-V_{GS} = 20\,V;\ V_{DS} = 0;\ T_{amb} = 150\,^{\circ}C$	$-I_{GSS}$	<	0.5	–	μA
$-V_{GS} = 15\,V;\ V_{DS} = 0;\ T_{amb} = 150\,^{\circ}C$	$-I_{GSS}$	<	–	0.5	μA
Drain cut-off current					
$V_{DS} = 15\,V;\ -V_{GS} = 10\,V$	I_{DSX}	<	0.25	0.25	nA
$V_{DS} = 15\,V;\ -V_{GS} = 10\,V;\ T_{amb} = 150\,^{\circ}C$	I_{DSX}	<	0.5	0.5	μA

			2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
Drain current [1]						
$V_{DS} = 15\,V;\ V_{GS} = 0$	I_{DSS}	>	50	20	8	mA
	I_{DSS}	<	–	100	80	mA

			2N4856 2N4857 2N4858	2N4859 2N4860 2N4861	
Gate-source breakdown voltage					
$-I_G = 1\,μA;\ V_{DS} = 0$	$-V_{(BR)GSS}$		40	30	V

			2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
Gate-source cut-off voltage						
$I_D = 0.5\ nA;\ V_{DS} = 15\,V$	$-V_{(P)GS}$	>	4	2	0.8	V
		<	10	6	4	V
Drain-source voltage (on)						
$I_D = 20\ mA;\ V_{GS} = 0$	V_{DSon}	<	0.75	–	–	V
$I_D = 10\ mA;\ V_{GS} = 0$	V_{DSon}	<	–	0.50	–	V
$I_D = 5\ mA;\ V_{GS} = 0$	V_{DSon}	<	–	–	0.50	V
Drain-source resistance (on) at $f = 1\,kHz$						
$I_D = 0;\ V_{GS} = 0$	r_{dson}	<	25	40	60	Ω

[1] measured under pulsed conditions: $t_p = 100\ ms;\ \delta \le 0.1$

y-parameters (common source)

$V_{DS} = 0$; $-V_{GS} = 10$ V; $f = 1$ MHz

Input capacitance	C_{is}	$<$		18	pF
Feedback capacitance	C_{rs}	$<$		8	pF

Switching times (see Figs 2 and 3)

$V_{DD} = 10$ V; $V_{GS} = 0$

			2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
Drain current	I_D	$=$	20	10	5	mA
Gate-source voltage (peak value)	$-V_{GSM}$	$=$	10	6	4	V
Delay time	t_d	$<$	6	6	10	ns
Rise time	t_r	$<$	3	4	10	ns
Turn-off time	t_{off}	$<$	25	50	100	ns
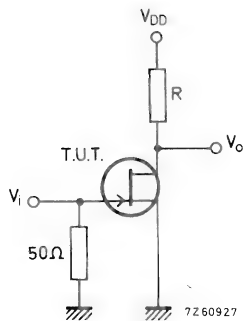
Fig. 2 Switching times test circuit.

2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
R = 464	953	1910	Ω

Pulse generator:

$t_r \leqslant$ 1 ns

$t_f \leqslant$ 1 ns

δ = 0,02

$Z_o =$ 50 Ω
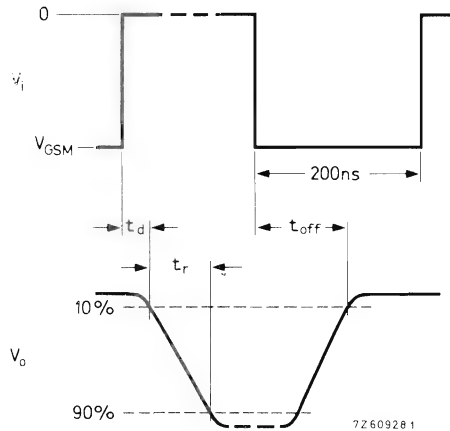
Fig. 3 Input and output waveforms.

Oscilloscope:

$t_r \leqslant 0,75$ ns

$R_i \geqslant$ 1 MΩ

$C_i \leqslant$ 2,5 pF

DEVICE DATA

MOS-FETS

single gate

N-CHANNEL INSULATED GATE MOS-FET

Depletion type field-effect transistor in a TO-72 metal envelope with the substrate connected to the case. It is intended for linear applications in the audio as well as the i.f. and v.h.f. frequency region, and in cases where high input impedance, low gate leakage currents and low noise figures are of importance.

QUICK REFERENCE DATA

Drain-substrate voltage	V_{DB}	max.	30	V
Gate-substrate voltage (continuous)	$\pm V_{GB}$	max.	10	V
Drain current $V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}		10 to 40	mA
Transfer admittance $I_D = 5$ mA; $V_{DS} = 15$ V; f = 1 kHz	$\lvert Y_{fs} \rvert$	>	6	mS
Feedback capacitance $I_D = 5$ mA; $V_{DS} = 15$ V; f = 1 MHz	C_{rs}	<	0,7	pF
Noise figure at f = 200 MHz $I_D = 5$ mA; $V_{DS} = 15$ V; $T_{amb} = 25$ °C $G_S = 1$ mS; $B_S = B_{Sopt}$	F	<	5	dB
Equivalent noise voltage at f = 1 kHz $I_D = 5$ mA; $V_{DS} = 15$ V; $T_{amb} = 25$ °C	$V_n/\sqrt{B}$	typ.	100	nV/$\sqrt{Hz}$

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.

(1) = substrate (b) connected to case

Accessories: 56246 (distance disc).

Note

To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber which should be removed just after the transistor is soldered into the circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-substrate voltage	V_{DB}	max.	30 V
Source-substrate voltage	V_{SB}	max.	30 V
Gate-substrate voltage (continuous)	$\pm V_{GB}$	max.	10 V
Repetitive peak gate to all other terminals voltage		max.	15 V
$V_{SB} = V_{DB} = 0$; $f > 100$ Hz	V_{G-N}	min.	-15 V
Drain current (d.c.)	I_D	max.	20 mA
Drain current (peak value) $t_p = 20$ ms; $\delta = 0{,}1$	I_{DM}	max.	50 mA
Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	200 mW
Storage temperature	T_{stg}		-65 to $+125$ °C
Junction temperature	T_j	max.	125 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	500 K/W

CHARACTERISTICS T_j = 25 $^{\circ}$C unless otherwise specified

Gate currents; V_{BS} = 0

$-V_{GS}$ = 10 V; V_{DS} = 0	$-I_{GSS}$	<	10	pA
V_{GS} = 10 V; V_{DS} = 0	I_{GSS}	<	10	pA
$-V_{GS}$ = 10 V; V_{DS} = 0; T_j = 125 $^{\circ}$C	$-I_{GSS}$	<	200	pA
V_{GS} = 10 V; V_{DS} = 0; T_j = 125 $^{\circ}$C	I_{GSS}	<	200	pA

Bulk currents; V_{GB} = 0

$-V_{BD}$ = 30 V; I_S = 0	$-I_{BDO}$	<	10	μA
$-V_{BS}$ = 30 V; I_D = 0	$-I_{BSO}$	<	10	μA

Drain current

V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	10 to 40	mA

Gate-source voltage

I_D = 100 nA; V_{DS} = 15 V	$-V_{GS}$	0.5 to 3.5	V

Gate-source cut-off voltage

I_D = 100 nA ; V_{DS} = 15 V	$-V_{(P)GS}$	<	4	V

y parameters T_{amb} = 25 $^{\circ}$C

I_D =   5 mA; V_{DS} = 15 V

Transfer admittance at f = 1 kHz	$|y_{fs}|$	>	6	mS
Output admittance at f = 1 kHz	$|y_{os}|$	<	0.4	mS
Input capacitance at f = 1 MHz	C_{is}	<	5	pF
Feedback capacitance at f = 1 MHz	C_{rs}	<	0.7	pF
Output capacitance at f = 1 MHz	C_{os}	<	3	pF

Noise figure at f = 200 MHz T_{amb} = 25 $^{\circ}$C

I_D = 5 mA; V_{DS} = 15 V

G_S = 1 mS; B_S = B_{Sopt}	F	<	5	dB

Equivalent noise voltage T_{amb} = 25 $^{\circ}$C

I_D = 5 mA; V_{DS} = 15 V; f = 120 Hz	$V_n/\sqrt{B}$	typ.	300	$nV/\sqrt{Hz}$
f = 1 kHz	$V_n/\sqrt{B}$	typ.	100	$nV/\sqrt{Hz}$
f = 10 kHz	$V_n/\sqrt{B}$	typ.	35	$nV/\sqrt{Hz}$

7Z62210

typical values
$V_{DS} = 15V$

I_D (mA)

$V_{GS} = +0.5V$

0V

-0.5V

-1V

-1.5V

T_j (°C)

7Z62208

$V_{DS} = 15V$
$V_{BS} = 0$
$f = 1kHz$
$T_{amb} = 25°C$

$|y_{os}|$ ($\mu A/V$)

typ

I_D (mA)

7Z62207

$V_{DS} = 15V$
$V_{BS} = 0$
$f = 1kHz$
$T_{amb} = 25°C$

$|y_{fs}|$ (mA/V)

typ

I_D (mA)

Top-left graph (7Z62075): g_{is} (μA/V) and b_{is} (mA/V) versus f (MHz). Curves labelled g_{is} and b_{is}.

typical values
$I_D = 5$mA
$V_{DS} = 15$V
$T_{amb} = 25°$C

Top-right graph (7Z62073): b_{rs} (μA/V) and $-C_{rs}$ (pF) versus f (MHz). Curves labelled $-C_{rs}$ and b_{rs}.

typical values
$I_D = 5$mA
$V_{DS} = 15$V
$T_{amb} = 25°$C

Bottom-left graph (7Z62072): g_{fs}, $-b_{fs}$ (mA/V) versus f (MHz). Curves labelled g_{fs} and $-b_{fs}$.

typical values
$I_D = 5$mA
$V_{DS} = 15$V
$T_{amb} = 25°$C

Bottom-right graph (7Z62074): g_{os} (μA/V) and b_{os} (mA/V) versus f (MHz). Curves labelled b_{os} and g_{os}.

typical values
$I_D = 5$mA
$V_{DS} = 15$V
$T_{amb} = 25°$C

7Z62209

typical values
$T_{amb} = 25°C$

$-C_{rs}$
(pF)

0.6

0.5

$V_{DS} = 5V$

0.4

15V

0.3

0.2
+ 2.5   0   -2.5 V_{GS}(V) - 5

7Z62225

typical values
$T_{amb} = 25°C$

C_{is}
(pF)

4

3

$V_{DS} =$
5V
15V

2

1

0
+ 2.5   0   -2.5 V_{GS}(V) - 5

MOSFET N-CHANNEL DEPLETION SWITCHING TRANSISTORS

Symmetrical insulated-gate silicon MOS field-effect transistor of the N-channel depletion mode type.

The transistor is sealed in a TO-72 envelope and features a low ON-resistance and low capacitances.

The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:
● analog and/or digital switch
● switch driver
● convertor
● chopper

QUICK REFERENCE DATA

			BSD10	BSD12	
Drain-source voltage	V_{DS}	max.	10	20	V
Gate-source voltage	V_{GS}	max.	+15 −30	+15 −40	V V
Drain current (d.c.)	I_D	max.		50	mA
Total power dissipation up to T_{amb} = 25 °C (free air)	P_{tot}	max.		275	mW
Junction temperature	T_j	max.		125	°C
Drain-source ON-resistance V_{GS} = 10 V; V_{SB} = 0; I_D = 1 mA	R_{DSon}	$<$		30	Ω
Feedback capacitance V_{GS} = V_{BS} = −5 V; V_{DS} = 10 V; f = 1 MHz	C_{rss}	typ.		0,6	pF

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.
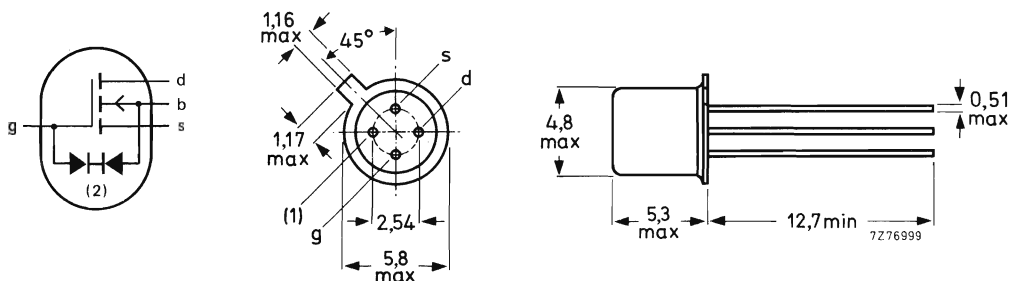
(1) Substrate (b) connected to case.

Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BSD10	BSD12	
Drain-source voltage	V_{DS}	max.	10	20	V
Source-drain voltage	V_{SD}	max.	10	20	V
Drain-substrate voltage	V_{DB}	max.	15	25	V
Source-substrate voltage	V_{SB}	max.	15	25	V
Gate-substrate voltage	V_{GB}	max.	+ 15 / −15	+ 15 / −15	V
Gate-source voltage	V_{GS}	max.	+ 15 / −30	+ 15 / −40	V
Drain current (d.c.)	I_D	max.	50		mA
Total power dissipation up to T_{amb} = 25 °C in free air	P_{tot}	max.	275		mW
Storage temperature	T_{stg}		−65 to + 150		°C
Junction temperature	T_j	max.	125		°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	360	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

			BSD10	BSD12	
Drain-source breakdown voltage $V_{GS} = V_{BS} = -5$ V; $I_S = 10$ nA	$V_{(BR)DSX}$	>	10	20	V
Source-drain breakdown voltage $V_{GD} = V_{BD} = -5$ V; $I_D = 10$ nA	$V_{(BR)SDX}$	>	10	20	V
Drain-substrate breakdown voltage $V_{GB} = 0$; $I_D = 10$ nA; open source	$V_{(BR)DBO}$	>	15	25	V
Source-substrate breakdown voltage $V_{GB} = 0$; $I_S = 10$ nA; open drain	$V_{(BR)SBO}$	>	15	25	V
Drain-source leakage current $V_{GS} = V_{BS} = -5$ V; $V_{DS} = 10$ V	I_{DSoff}	typ.	1,0		nA
Source-drain leakage current $V_{GD} = V_{BD} = -5$ V; $V_{SD} = 10$ V	I_{SDoff}	typ.	1,0		nA
Gate-substrate leakage current $V_{DB} = V_{SB} = 0$; $V_{GB} = \pm 15$ V	I_{GBS}	<	10		nA
Forward transconductance at f = 1 kHz $V_{DS} = 10$ V; $V_{SB} = 0$; $I_S = 20$ mA	g_{fs}	> / typ.	10 / 15		mS / mS

Gate-source cut-off voltage
$V_{DS} = 10$ V; $V_{SB} = 0$;
$I_D = 10$ μA

$-V_{(P)GS} <$		2,0	V

Drain-source ON-resistance
$I_D = 1$ mA; $V_{SB} = 0$
$V_{GS} = 5$ V

r_{DSon}	typ.	25	Ω
	$<$	50	Ω

$V_{GS} = 10$ V

r_{DSon}	typ.	15	Ω
	$<$	30	Ω

Capacitances at f = 1 MHz (see Fig. 2)
$V_{GS} = V_{BS} = -5$ V; $V_{DS} = 10$ V

Feed-back capacitance	C_{rss}	typ.	0,6	pF
Input capacitance	C_{iss}	typ.	2,3	pF
Output capacitance	C_{oss}	typ.	1,9	pF

Switching times (see Fig. 3)
$V_{DD} = 10$ V; $V_i = -5$ to $+5$ V

t_{on}	typ.	1,0	ns
t_{off}	typ.	5,0	ns

7Z90791

Fig. 2 Capacitances model.
$C_{iss} = C_{gs} + C_{gd} + C_{gb}$
$C_{oss} = C_{gd} + C_{bd}$
$C_{rss} = C_{gd}$

7Z90790

7Z87626

Fig. 3 Switching times and input and output waveforms;
$R_i = 50$ Ω; $t_r < 0,5$ ns; $t_f < 1,0$ ns; $t_p = 20$ ns; $\delta < 0,01$.

MOSFET N-CHANNEL DEPLETION SWITCHING TRANSISTORS

Symmetrical insulated-gate silicon MOS field-effect transistors of the N-channel depletion mode type.

The transistor is sealed in a SOT-143 envelope and features a low ON-resistance and low capacitances.

The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:
- analog and/or digital switch
- switch driver
- convertor
- chopper

QUICK REFERENCE DATA

			BSD20	BSD22	
Drain-source voltage	V_{DS}	max.	10	20	V
Gate-source voltage	V_{GS}	max.	$+15$ -30	$+15$ -40	V V
Drain current (d.c.)	I_D	max.		50	mA
Total power dissipation up to $T_{amb} = 25\,^{\circ}C$	P_{tot}	max.		230	mW
Junction temperature	T_j	max.		125	$^{\circ}C$
Drain-source ON-resistance $V_{GS} = 10$ V; $V_{SB} = 0$; $I_D = 1$ mA	R_{DSon}	<		30	Ω
Feed-back capacitance $V_{GS} = V_{BS} = -5$ V; $V_{DS} = 10$ V; f = 1 MHz	C_{rss}	typ.		0,6	pF

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-143.

Pinning;
1 = substrate (b)
2 = source
3 = drain
4 = gate
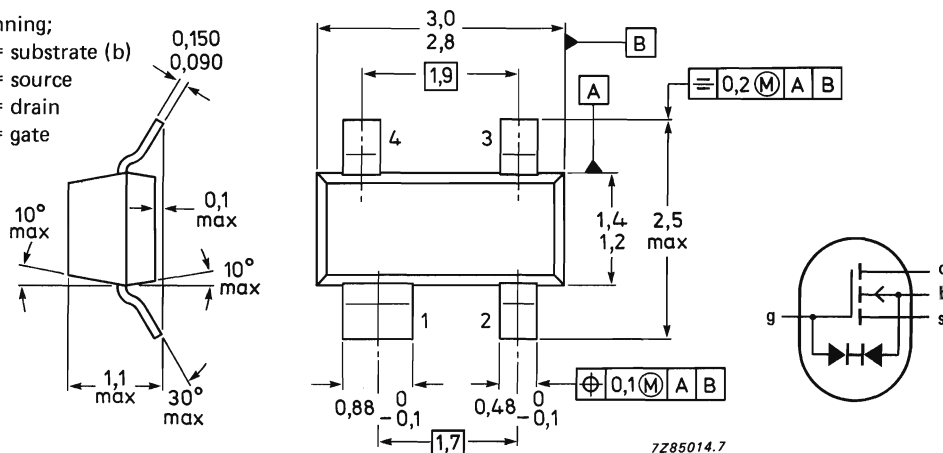
TOP VIEW

7Z85014.7

Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BSD20	BSD22	
Drain-source voltage	V_{DS}	max.	10	20	V
Source-drain voltage	V_{SD}	max.	10	20	V
Drain-substrate voltage	V_{DB}	max.	15	25	V
Source-substrate voltage	V_{SB}	max.	15	25	V
Gate-substrate voltage	V_{GB}	max.	± 15	± 25	V
Gate-source voltage	V_{GS}	max.	$+15$ -30	$+15$ -40	V V
Drain current (d.c.)	I_D	max.	50		mA
Total power dissipation up to $T_{amb} = 25\ ^{o}C^*$	P_{tot}	max.	230		mW
Storage temperature	T_{stg}		-65 to $+150$		^{o}C
Junction temperature	T_j	max.	125		^{o}C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j\text{-}a}$	$=$	430	K/W

CHARACTERISTICS

$T_{amb} = 25\ ^{o}C$ unless otherwise specified

			BSD20	BSD22	
Drain-source breakdown voltage $V_{GS} = V_{BS} = -5\ V; I_S = 10\ nA$	$V_{(BR)DSX}$	$>$	10	20	V
Source-drain breakdown voltage $V_{GD} = V_{BD} = -5\ V; I_D = 10\ nA$	$V_{(BR)SDX}$	$>$	10	20	V
Drain-substrate breakdown voltage $V_{GB} = 0; I_D = 10\ nA;$ open source	$V_{(BR)DBO}$	$>$	15	25	V
Source-substrate breakdown voltage $V_{GB} = 0; I_S = 10\ nA;$ open drain	$V_{(BR)SBO}$	$>$	15	25	V
Drain-source leakage current $V_{GS} = V_{BS} = -5\ V; V_{DS} = 10V$	I_{DSoff}	typ.	1,0		nA
Source-drain leakage current $V_{GD} = V_{BD} = 5\ V; V_{SD} = 10V$	I_{SDoff}	typ.	1,0		nA
Gate-substrate leakage current $V_{DB} = V_{SB} = 0; V_{GB} = \pm 15\ V$	I_{GBS}	$<$	10		nA

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

Forward transconductance at f = 1 kHz
  V_{DS} = 10 V; V_{SB} = 0; I_D = 20 mA

g_{fs}	>	10	mS
	typ.	15	mS

Gate-source cut-off voltage
  V_{DS} = 10 V; V_{SB} = 0; I
  I_D = 10 μA

$-V_{(P)GS}$ < 2,0 V ←

Drain-source ON-resistance
  I_D = 1 mA; V_{SB} = 0;
  V_{GS} = 5 V

R_{DSon}	typ.	25	Ω
	<	50	Ω

  V_{GS} = 10 V

R_{DSon}	typ.	15	Ω
	<	30	Ω

Capacitances at f = 1 MHz
  V_{GS} = V_{BS} = −5V; V_{DS} = 10 V
  Feed-back capacitance

  C_{rss} typ.   0,6 pF

  Input capacitance C_{iss} typ.   1,5 pF

  Output capacitance C_{oss} typ.   1,0 pF

Switching times (see Fig. 3)
  V_{DD} = 10 V; V_i = −5 V to +5 V

t_{on}	typ.	1,0	ns ←
t_{off}	typ.	5,0	ns

7Z90791

Fig. 2 Capacitances model.

C_{iss} = C_{gs} + C_{gd} + C_{gb}

C_{oss} = C_{gd} + C_{bd}

C_{rss} = C_{gd}

7Z90790

7Z87626

Fig. 3 Switching times and input and output waveforms;
R_i = 50 Ω; t_r < 0,5 ns; t_f < 1,0 ns; t_p = 20 ns; δ < 0,01.

MOSFET N-CHANNEL ENHANCEMENT SWITCHING TRANSISTORS

Symmetrical insulated gate silicon MOS field-effect transistor of the N-channel enhancement mode type.

These transistors are hermetically sealed in a TO-72 envelope and feature a low ON-resistance, high switching speed and low capacitances.

The types BSD213 and BSD215 are protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:
- analogue and/or digital switch
- switch driver
- converters
- choppers

QUICK REFERENCE DATA

			BSD212	BSD213	BSD214	BSD215	
Drain-source voltage	V_{DS}	max.	10	10	20	20	V
Gate-source voltage	V_{GS}	max.	± 40	+ 15 −30	± 40	+ 15 −40	V
Drain current (d.c.)	I_D	max.		50			mA
Total power dissipation up to $T_{amb} = 25\,^{\circ}C$ (free air)	P_{tot}	max.		¨275			mW
Drain-source resistance $I_D = 1$ mA; $V_{SB} = 0$; $V_{GS} = 15$ V	$R_{DS(on)}$	typ.		25			Ω
Feedback capacitance $V_{GS} = V_{BS} = -15$ V; $V_{DS} = 10$ V; $f = 1$ MHz	C_{rss}	typ.		0,6			pF
Junction temperature	T_j	max.		125			$^{\circ}C$

MECHANICAL DATA

See next page.

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.

1,16 max   45°

s
d

1,17 max

4,8 max

0,51 max

5,3 max   12,7 min   7Z76999

(1) g   2,54

5,8 max

d
b
g   s
(2)
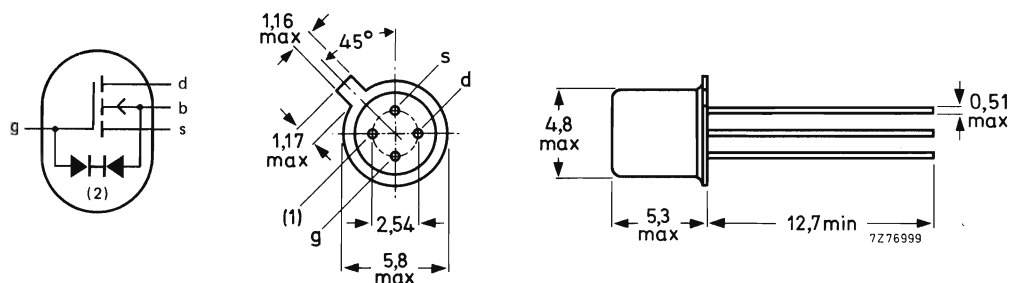
(1) Substrate (b) connected to case.
(2) Diode protection on types BSD213 and BSD215 only.
BSD212 and BSD214 have no protection diode.
To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber which should be removed just after the transistor is soldered into the circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BSD212	BSD213	BSD214	BSD215	
Drain-source voltage	V_{DS}	max.	10	10	20	20	V
Source-drain voltage	V_{SD}	max.	10	10	20	20	V
Drain-substrate voltage	V_{DB}	max.	15	15	25	25	V
Source-substrate voltage	V_{SB}	max.	15	15	25	25	V
Gate-substrate voltage	V_{GB}	max.	± 40	± 15	± 40	± 15	V
Gate-source voltage	V_{GS}	max.	± 40	+ 15 −30	± 40	+ 15 −40	V
Gate-drain voltage	V_{GD}	max.	± 40	+ 15 −30	± 40	+ 15 −40	V
Drain current (d.c.)	I_D	max.	50				mA
Total power dissipation up to T_{amb} = 25 °C (free air)	P_{tot}	max.	275				mW
Storage temperature range	T_{stg}		−65 to + 175				°C
Junction temperature	T_j	max.	125				°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	360	K/W

CHARACTERISTICS

T_{amb} = 25 ^oC unless otherwise specified

			BSD212	BSD213	BSD214	BSD215	
Drain-source breakdown voltage $V_{GS} = V_{BS} = -5$ V; $I_S = 10$ nA	$V_{(BR)DSX}$ >		10	10	20	20	V
Source-drain breakdown voltage $V_{GD} = V_{BD} = -5$ V; $I_D = 10$ nA	$V_{(BR)SDX}$ >		10	10	20	20	V
Drain-substrate breakdown voltage $V_{GB} = 0$; $I_D = 10$ nA; open source	$V_{(BR)DBO}$ >		15	15	25	25	V
Source-substrate breakdown voltage $V_{GB} = 0$; $I_S = 10$ nA; open drain	$V_{(BR)SBO}$ >		15	15	25	25	V
Drain-source leakage current $V_{GS} = V_{BS} = -5$ V; $V_{DS} = 10$ V	I_{DSoff}	typ.	1,0	1,0	—	—	nA
$V_{GS} = V_{BS} = -5$ V; $V_{DS} = 20$ V	I_{DSoff}	typ.	—	—	1,0	1,0	nA
Source-drain leakage current $V_{GD} = V_{BD} = -5$ V; $V_{SD} = 10$ V	I_{SDoff}	typ.	1,0	1,0	—	—	nA
$V_{GD} = V_{BD} = -5$ V; $V_{SD} = 20$ V	I_{SDoff}	typ.	—	—	1,0	1,0	nA
Gate-substrate leakage current $V_{DB} = V_{SB} = 0$; $V_{GB} = \pm 40$ V	I_{GBS} <		0,1	—	0,1	—	nA
$V_{DB} = V_{SB} = 0$; $V_{GB} = \pm 15$ V	I_{GBS} <		—	10	—	10	nA
Threshold voltage $V_{DS} = V_{GS} = V_{GS(th)}$ $V_{SB} = 0$; $I_S = 1$ μA	$V_{GS(th)}$		0,1 to 2,0				V

			BSD212	BSD213	BSD214	BSD215	
Drain-source resistance $I_D = 1,0$ mA; $V_{SB} = 0$; $V_{GS} = 5$ V	$R_{DS(on)}$	typ. <	50 70	50 70	50 70	50 70	Ω Ω
$V_{GS} = 10$ V	$R_{DS(on)}$	typ. <	30 45	30 45	30 45	30 45	Ω
$V_{GS} = 15$ V	$R_{DS(on)}$	typ.	25	25	25	25	Ω
$V_{GS} = 25$ V	$R_{DS(on)}$	typ.	15		15		Ω

DYNAMIC CHARACTERISTICS

Forward transconductance at f = 1 kHz $V_{DS} = 10$ V; $V_{SB} = 0$; $I_D = 20$ mA	g_{fs}	typ. >	15 10	mS
Capacitance at f = 1 MHz (see Fig. 2) $V_{GS} = V_{BS} = -15$ V; $V_{DS} = 10$ V				
Feed-back capacitance	C_{rss}	typ.	0,6	pF
Input capacitance	C_{iss}	typ.	2,3	pF
Output capacitance	C_{oss}	typ.	1,9	pF

DYNAMIC CHARACTERISTICS (continued)
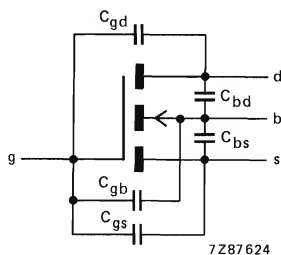
Fig. 2 Capacitances model.

$C_{iss} = C_{GS} + C_{GD} + C_{GB}$

$C_{oss} = C_{GD} + C_{BD}$

$C_{rss} = C_{GD}$

Switching times (see Fig. 3)

$V_{DD} = 10$ V; $V_i = -5$ V to +5 V

t_{on}	typ.		1,0	ns
t_{off}	typ.		5,0	ns
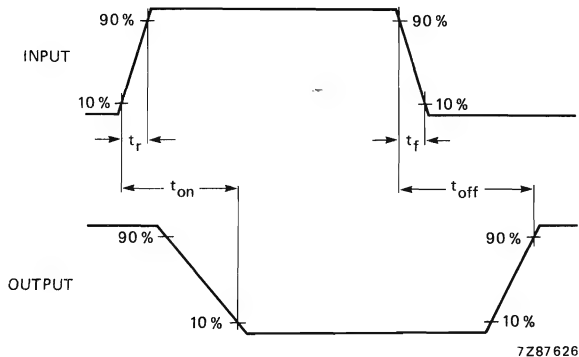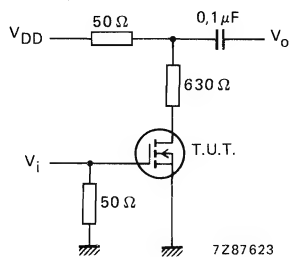
Fig. 3 Switching times test circuit and input and output waveforms.

Pulse generator:

$R_i = 50$ Ω

$t_r < 0,5$ ns

$t_f < 1,0$ ns

$t_p = 20$ ns

$\delta < 0,01$

MOSFET N-CHANNEL ENHANCEMENT SWITCHING TRANSISTOR

Symmetrical insulated-gate silicon MOS field-effect transistor of the N-channel enhancement mode type.

The transistor is sealed in a SOT-143 envelope and features a low ON resistance and low capacitances.

The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:
- analog and/or digital switch
- switch driver

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	10	V
Source-drain voltage	V_{SD}	max.	10	V
Drain-substrate voltage	V_{DB}	max.	15	V
Source-substrate voltage	V_{SB}	max.	15	V
Drain current (d.c.)	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	230	mW
Gate-source cut-off voltage $V_{DS} = V_{GS}$; $V_{SB} = 0$; $I_D = 1\ \mu A$	$V_{(P)GS}$	$>$ $<$	0,1 2,0	V V
Drain-source ON-resistance $V_{GS} = 10$ V; $V_{SB} = 0$; $I_D = 0,1$ mA	$R_{DS(on)}$	$<$	45	Ω
Feed-back capacitance $V_{GS} = V_{BS} = -15$ V; $V_{DS} = 10$ V; f = 1 MHz	C_{rss}	typ.	0,6	pF

MECHANICAL DATA
SOT-143 (see Fig. 1).

See also *Soldering recommendations*.

Fig. 1 SOT-143.

Dimensions in mm

0,150
0,090

3,0
2,8

1,9

B

A

0,2 (M) A B

Marking code:

BSS83 = M74

10°
max

0,1
max

10°
max

1,4
1,2

2,5
max

1,1
max

30°
max

0,88 $0_{-0,1}$ 0,48 $0_{-0,1}$

1,7

0,1 (M) A B

7Z85014.7

TOP VIEW

Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	10	V
Source-drain voltage	V_{SD}	max.	10	V
Drain-substrate voltage	V_{DB}	max.	15	V
Source-substrate voltage	V_{SB}	max.	15	V
Drain current (d.c.)	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	230	mW*
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	125	°C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j\text{-}a}$	=	430	K/W*

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Drain-source breakdown voltage $V_{GS} = V_{BS} = -5$ V; $I_D = 10$ nA	$V_{(BR)DSX}$	>	10	V
Source-drain breakdown voltage $V_{GD} = V_{BD} = -5$ V; $I_D = 10$ nA	$V_{(BR)SDX}$	>	10	V
Drain-substrate breakdown voltage $V_{GB} = 0$; $I_D = 10$ nA; open source	$V_{(BR)DBO}$	>	15	V
Source-substrate breakdown voltage $V_{GB} = 0$; $I_D = 10$ nA; open drain	$V_{(BR)SBO}$	>	15	V
Drain-source leakage current $V_{GS} = V_{BS} = -2$ V; $V_{DS} = 6,6$ V	I_{DSoff}	<	10	nA

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

Source-drain leakage current
$V_{GD} = V_{BD} = -2$ V; $V_{SD} = 6,6$ V

I_{SDoff}	<	10 nA ←

Forward transconductance at f = 1 kHz
$V_{DS} = 10$ V; $V_{SB} = 0$; $I_D = 20$ mA

g_{fs}	>	10 mS
	typ.	15 mS

Gate-source cut-off voltage
$V_{DS} = V_{GS}$; $V_{SB} = 0$; $I_D = 1$ μA

$V_{(P)GS}$	>	0,1 V
	<	2,0 V

Drain-source ON-resistance
$I_D = 0,1$ mA;

$V_{GS} = 5$ V; $V_{SB} = 0$

$R_{DS(on)}$	<	70 Ω

$V_{GS} = 10$ V; $V_{SB} = 0$

$R_{DS(on)}$	<	45 Ω

$V_{GS} = 3,2$ V; $V_{SB} = 6,8$ V (see Fig. 4)

$R_{DS(on)}$	typ.	80 Ω
	<	120 Ω

Gate-substrate zener voltages
$V_{DB} = V_{SB} = 0$; $-I_C = 10$ μA
$V_{DB} = V_{SB} = 0$; $+I_G = 10$ μA

$V_{Z(1)}$	>	12,5 V
$V_{Z(2)}$	>	12,5 V

Capacitances at f = 1 MHz
$V_{GS} = V_{BS} = -15$ V; $V_{DS} = 10$ V

Feed-back capacitance

Input capacitance

Output capacitance

C_{rss}	typ.	0,6 pF
C_{iss}	typ.	1,5 pF
C_{oss}	typ.	1,0 pF

Switching times (see Fig. 2)
$V_{DD} = 10$ V; $V_i = 5$ V

t_{on}	typ.	1,0 ns
t_{off}	typ.	5,0 ns

Pulse generator:
R_i = 50 Ω
t_r < 0,5 ns
t_f < 1,0 ns
t_p = 20 ns
δ < 0,01
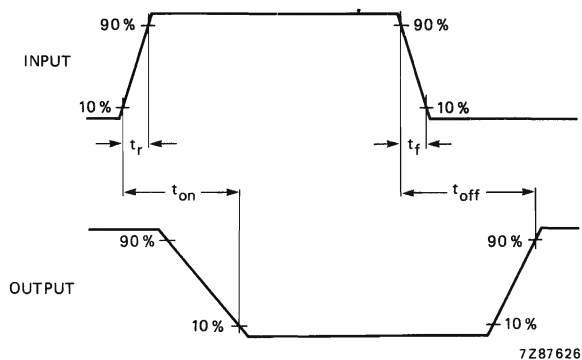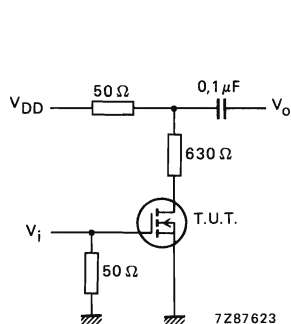
Fig. 2 Switching times test circuit and input and output waveforms.
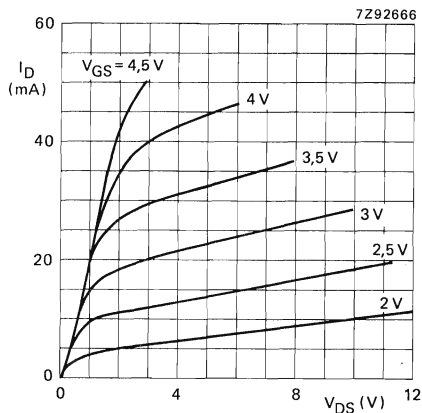
Fig. 3 V_{SB} = 0; typical values.
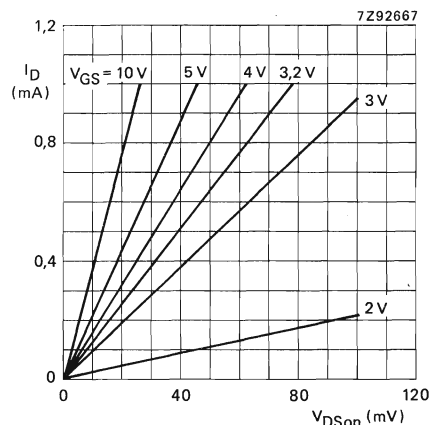
Fig. 4 V_{SB} = 6,8 V; typical values.
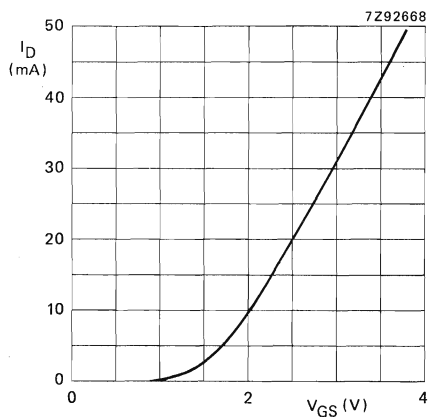
Fig. 5 V_{DS} = 10 V; V_{BS} = 0; typical values.
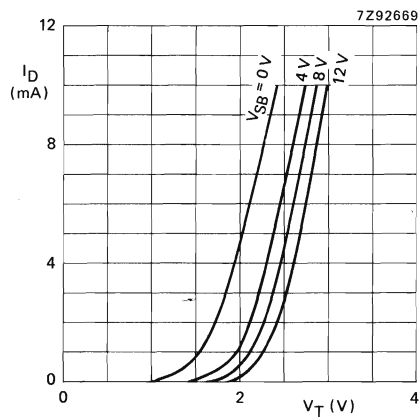
Fig. 6 V_{DS} = V_{GS} = V_T.
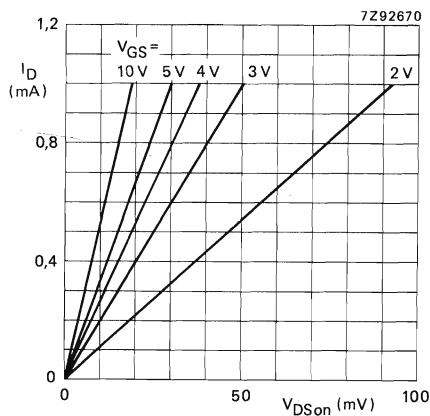
Fig. 7 V_{SB} = 0; typical values.

Conditions for Figs 3, 4, 5, 6 and 7:
T_j = 25 °C.

N-CHANNEL IG-MOS-FET

Symmetrical depletion type field-effect transistor in a TO-72 metal envelope with the substrate connected to the case. It is intended for chopper and other special switching applications, e.g. timing circuits, multiplex circuits, etc. The features are a very low drain-source 'on' resistance, a very high drain-source 'off' resistance and low feedback capacitances.

QUICK REFERENCE DATA

Drain-source resistance (on) at f = 1 kHz				
$V_{DS} = 0$; $V_{GS} = 5$ V; $V_{BS} = 0$	$r_{ds\ on}$	<	50	Ω
Drain-source resistance (off)				
$V_{DS} = 10$ V; $-V_{GS} = 5$ V; $V_{BS} = 0$	r_{DSoff}	>	10	$G\Omega$
Feedback capacitance at f = 1 MHz				
$-V_{GS} = 5$ V; $V_{DS} = 0$; $I_B = 0$	C_{rs}	<	0,5	pF
$-V_{GD} = 5$ V; $V_{SD} = 0$; $I_B = 0$	C_{rd}	<	0,5	pF

MECHANICAL DATA   Dimensions in mm

Fig. 1 TO-72.

(1) = substrate connected to case.

Accessories: 56246 (distance disc).

Note

To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber which should be removed just after the transistor is soldered into the circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-substrate voltage	V_{DB}	max.	30	V
Source-substrate voltage	V_{SB}	max.	30	V
Gate-substrate voltage (continuous)	V_{GB}	max.	10	V
		min.	−10	V
Repetitive peak gate to all other terminals voltage		max.	15	V
$V_{SB} = V_{DB} = 0; f > 100$ Hz	V_{G-N}	min.	−15	V
Non-repetitive peak gate to all other terminals voltage		max.	50	V
$V_{SB} = V_{DB} = 0; t < 10$ ms	V_{G-N}	min.	−50	V
Drain current (d.c.)	I_D	max.	25	mA
Drain current (peak value) $t_r = 20$ ms; $\delta = 0,1$	I_{DM}	max.	50	mA
Source current (peak value) $t_r = 20$ ms; $\delta = 0,1$	I_{SM}	max.	50	mA
Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	200	mW
Storage temperature	T_{stg}	−65 to + 125		°C
Junction temperature	T_j	max.	125	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\,j-a}$	=	0,5	°C/mW

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Drain cut-off currents; $V_{BS} = 0$

$V_{DS} = 10$ V; $-V_{GS} = 5$ V	I_{DSX}	<	1	nA
$V_{DS} = 10$ V; $-V_{GS} = 5$ V; $T_j = 125\ ^oC$	I_{DSX}	<	1	μA

Source cut-off currents; $V_{BD} = 0$

$V_{SD} = 10$ V; $-V_{GD} = 5$ V	I_{SDX}	<	1	nA
$V_{SD} = 10$ V; $-V_{GD} = 5$ V; $T_j = 125\ ^oC$	I_{SDX}	<	1	μA

Gate currents; $V_{BS} = 0$

$-V_{GS} = 10$ V; $V_{DS} = 0$	$-I_{GSS}$	<	10	pA
$V_{GS} = 10$ V; $V_{DS} = 0$	I_{GSS}	<	10	pA
$-V_{GS} = 10$ V; $V_{DS} = 0$; $T_j = 125\ ^oC$	$-I_{GSS}$	<	200	pA
$V_{GS} = 10$ V; $V_{DS} = 0$; $T_j = 125\ ^oC$	I_{GSS}	<	200	pA

Bulk currents; $V_{GB} = 0$

$-V_{BD} = 30$ V; $I_S = 0$	$-I_{BDO}$	<	10	μA
$-V_{BS} = 30$ V; $I_D = 0$	$-I_{BSO}$	<	10	μA

Drain-source resistance (on) at $f = 1$ kHz; $V_{BS} = 0$

$V_{GS} = 0$; $V_{DS} = 0$	r_{dson}	<	100	Ω
$V_{GS} = 0$; $V_{DS} = 0$; $T_j = 125\ ^oC$	r_{dson}	<	150	Ω
$+V_{GS} = 5$ V; $V_{DS} = 0$	r_{dson}	<	50	Ω

Drain-source resistance (off)

$-V_{GS} = 5$ V; $V_{DS} = 10$ V; $V_{BS} = 0$	r_{DSoff}	>	10	$G\Omega$

Feedback capacitances at $f = 1$ MHz

$-V_{GS} = 5$ V; $V_{DS} = 0$; $I_B = 0$	C_{rs}	<	0,5	pF
$-V_{GD} = 5$ V; $V_{SD} = 0$; $I_B = 0$	C_{rd}	<	0,5	pF

Gate to all other terminals capacitance at $f = 1$ MHz

$-V_{GB} = 5$ V; $V_{SB} = V_{DB} = 0$	C_{g-n}	<	6	pF
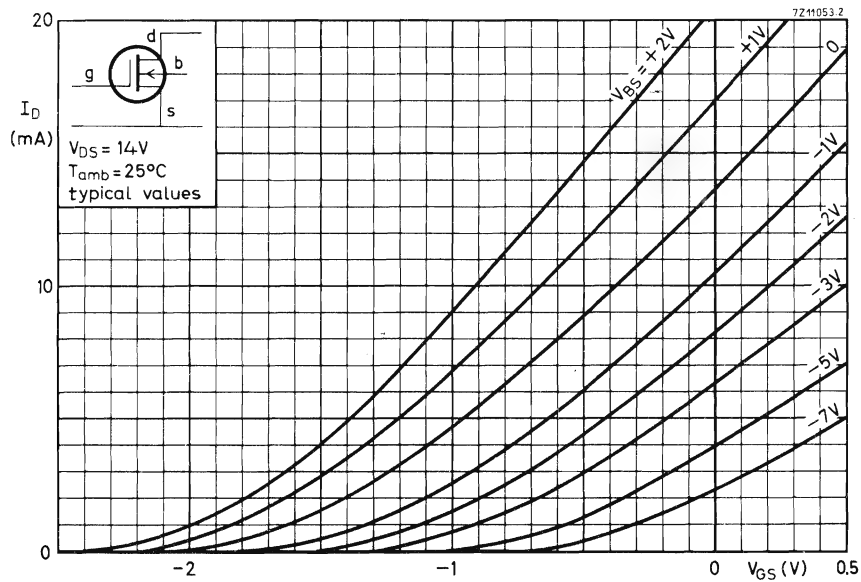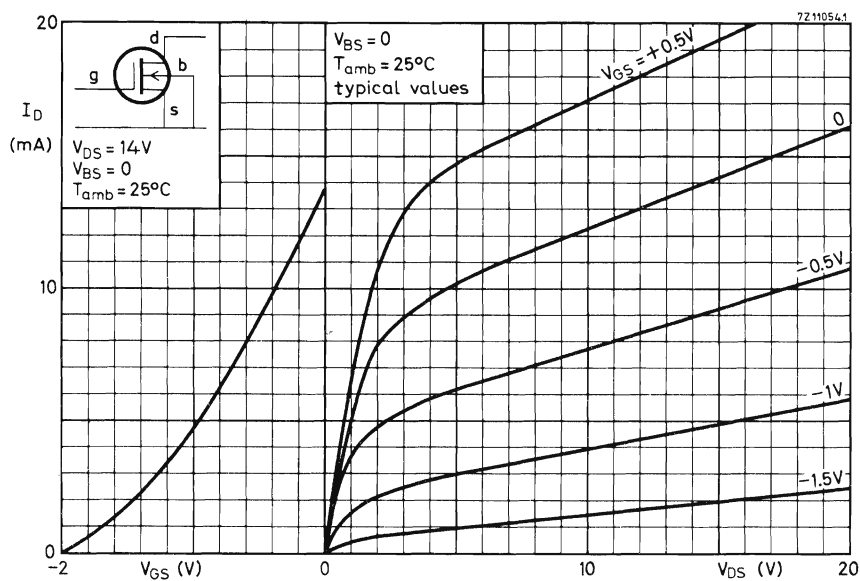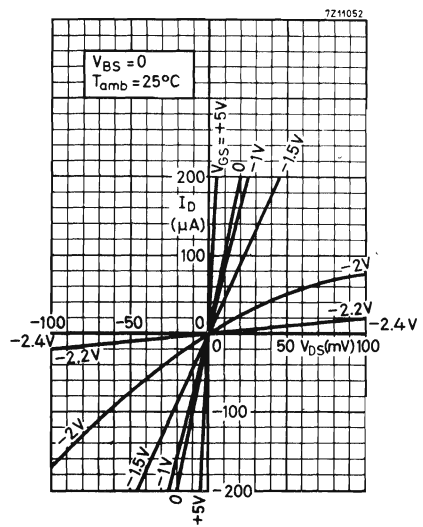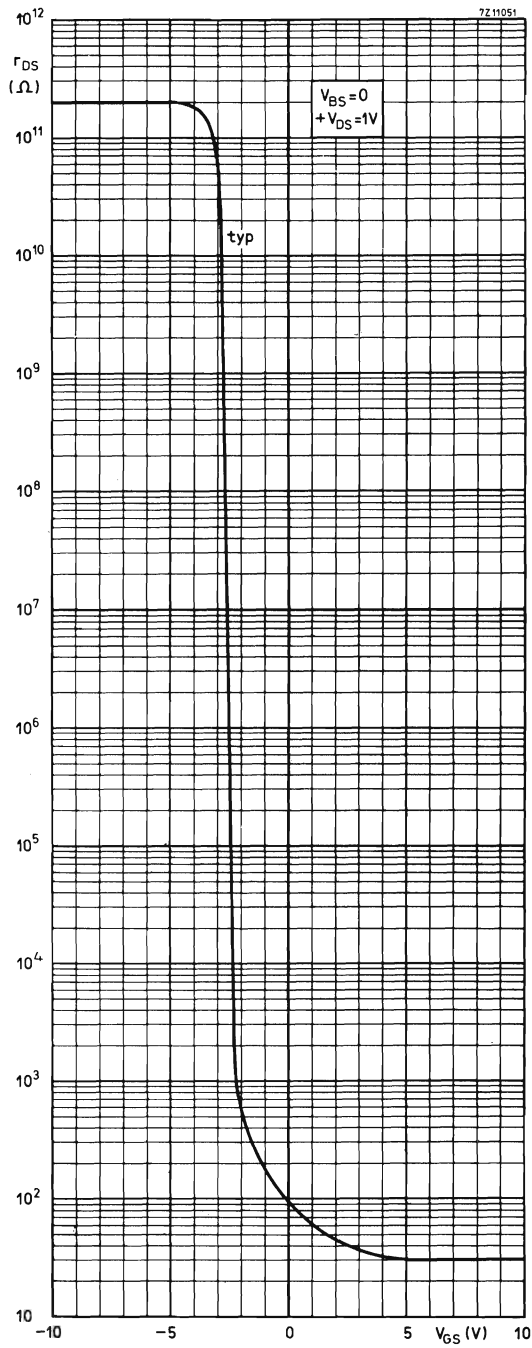
DEVICE DATA

MOS-FETS

dual gate

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for use in u.h.f. applications in television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.
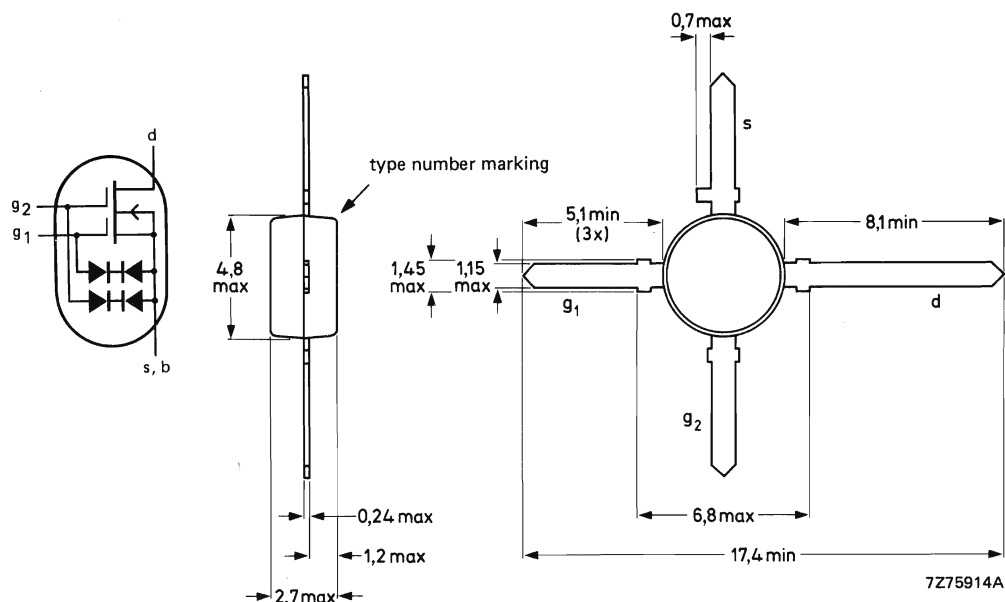
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current (peak value)	I_{DM}	max.	30	mA
Total power dissipation up to T_{amb} = 75 ^oC	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	^oC
Transfer admittance at f = 1 kHz I_D = 7 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$|y_{fs}|$	typ.	12	mS
Feedback capacitance at f = 1 MHz I_D = 7 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{rs}	typ.	25	fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 7 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; f = 800 MHz	F	typ.	2,8	dB
Power gain at f = 800 MHz I_D = 7 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; G_S = 2 mS; B_S = B_S opt; G_L = 1 mS; B_L = B_L opt	G_p	typ.	16,5	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.

type number marking

7Z75914

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (d.c. or average)	I_D	max.	20 mA
Drain current (peak value)	I_{DM}	max.	30 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Storage temperature	T_{stg}	−65 to +150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air
   mounted on the printed-circuit board $R_{th\,j-a}$ =   335 K/W

Dimensions in mm

(1) Connection made by
    a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_{amb} = 25 ^{o}C

Gate cut-off currents

$\pm V_{G1-S}$ = 5 V; V_{G2-S} = V_{DS} = 0	$\pm I_{G1-SS}$	<	50	nA
$\pm V_{G2-S}$ = 5 V; V_{G1-S} = V_{DS} = 0	$\pm I_{G2-SS}$	<	50	nA

Gate-source breakdown voltages

$\pm I_{G1-SS}$ = 10 mA; V_{G2-S} = V_{DS} = 0	$\pm V_{(BR)G1-SS}$	6,0 to 20	V
$\pm I_{G2-SS}$ = 10 mA; V_{G1-S} = V_{DS} = 0	$\pm V_{(BR)G2-SS}$	6,0 to 20	V

Drain current*

V_{DS} = 10 V; V_{G1-S} = 0; + V_{G2-S} = 4 V	I_{DSS}	2 to 20	mA

Gate-source cut-off voltages

I_D = 20 μA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	<	2,7	V
I_D = 20 μA; V_{DS} = 10 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	<	2,7	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 7 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; T_{amb} = 25 ^{o}C

Transfer admittance at f = 1 kHz	$|y_{fs}|$	>	9,5	mS
		typ.	12	mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	1,8	pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1,0	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0,9	pF
Noise figure at G_S = 2 mS; B_S = B_S opt				
f = 200 MHz	F	typ.	1,6	dB
f = 800 MHz	F	typ.	2,8	dB
Power gain at G_S = 2 mS; B_S = B_S opt				
G_L = 0,5 mS; B_L = B_L opt; f = 200 MHz	G_p	typ.	23	dB
G_L = 1 mS; B_L = B_L opt; f = 800 MHz	G_p	typ.	16,5	dB

* Measured under pulse conditions.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for v.h.f. applications in television tuners, especially in r.f. stages and mixer stages in S-channel tuners. The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain-current	I_D	max.	30	mA
Total power dissipation up to $T_{amb} = 75\ ^{o}C$	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	^{o}C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V	$|y_{fs}|$	typ.	17	mS
Feedback capacitance at f = 1 MHz I_D = 10 mA, V_{DS} = 15 V; + V_{G2-S} = 4 V	C_{rs}	typ.	25	fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V; f = 200 MHz	F	typ.	1,5	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain-current (d.c. or average)	I_D	max.	30	mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to $T_{amb} = 75\ ^oC$	P_{tot}	max.	225	mW
Storage temperature	T_{stg}	−65 to +150		^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to ambient in free air
mounted on the printed-circuit board (see Fig. 2) $R_{th\ j\text{-}a}$ = 335 K/W

Dimensions in mm

(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_{amb} = 25 °C

Gate cut-off currents

$\pm V_{G1-S}$ = 5 V; V_{G2-S} = V_{DS} = 0	$\pm I_{G1-SS}$	<	50 nA
$\pm V_{G2-S}$ = 5 V; V_{G1-S} = V_{DS} = 0	$\pm I_{G2-SS}$	<	50 nA

Gate-source breakdown voltages

$\pm I_{G1-SS}$ = 10 mA; V_{G2-S} = V_{DS} = 0	$\pm V_{(BR)G1-SS}$		6,0 to 20 V
$\pm I_{G2-SS}$ = 10 mA; V_{G1-S} = V_{DS} = 0	$\pm V_{(BR)G2-SS}$		6,0 to 20 V

Drain current*

V_{DS} = 15 V; V_{G1-S} = 0; + V_{G2-S} = 4 V	I_{DSS}		2 to 20 mA

Gate-source cut-off voltages

I_D = 20 μA; V_{DS} = 15 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	<	2,5 V
I_D = 20 μA; V_{DS} = 15 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	<	2,0 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source); I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert Y_{fs} \rvert$	> typ.	15 mS 17 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ. <	2,5 pF 3,0 pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1,2 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ. <	25 fF 35 fF
Output capacitance at f = 1 MHz	C_{os}	typ. <	1,0 pF 1,3 pF
Noise figure at G_S = 2 mS; B_S = B_S opt f = 200 MHz	F	typ. <	1,5 dB 2,8 dB
Power gain at G_S = 2 mS; B_S = B_S opt G_L = 0,5 mS; B_L = B_L opt; f = 200 MHz	G_p	typ.	25 dB

* Measured under pulse conditions.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for v.h.f. applications in television tuners. The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.
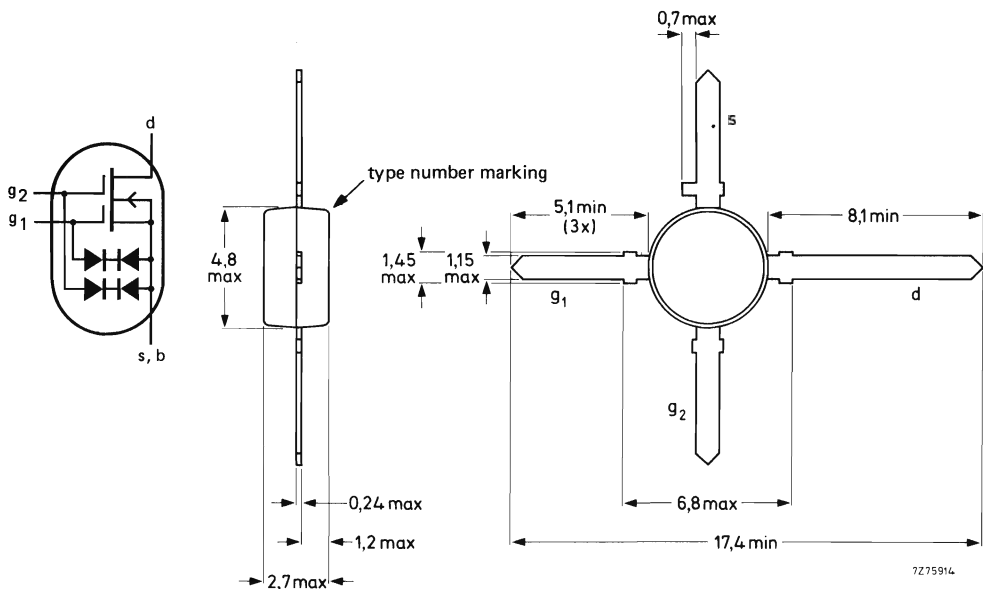
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain-current	I_D	max.	50	mA
Total power dissipation up to $T_{amb} = 75\ ^oC$	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	^oC
Transfer admittance at f = 1 kHz $I_D = 10$ mA; $V_{DS} = 15$ V; $+ V_{G2-S} = 4$ V	$|y_{fs}|$	typ.	18	mS
Feedback capacitance at f = 1 MHz $I_D = 10$ mA; $V_{DS} = 15$ V; $+ V_{G2-S} = 4$ V	C_{rs}	typ.	25	fF
Noise figure at $G_S = 2$ mS ; $B_S = B_S$ opt $I_D = 10$ mA; $V_{DS} = 15$ V; $+ V_{G2-S} = 4$ V; f = 200 MHz	F	typ.	1,0	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.

7Z75914A

BF964S

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain-current (d.c. or average)	I_D	max.	50	mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to $T_{amb} = 75\ ^oC$	P_{tot}	max.	225	mW
Storage temperature	T_{stg}	-65 to $+150$		^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to ambient in free air
  mounted on the printed-circuit board (see Fig. 2) $R_{th\,j\text{-}a}$ = 335 K/W

Dimensions in mm

(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_{amb} = 25 °C

Gate cut-off currents				
$\pm V_{G1-S}$ = 5 V; V_{G2-S} = V_{DS} = 0	$\pm I_{G1-SS}$	$<$	50	nA
$\pm V_{G2-S}$ = 5 V; V_{G1-S} = V_{DS} = 0	$\pm I_{G2-SS}$	$<$	50	nA
Gate-source breakdown voltages				
$\pm I_{G1-SS}$ = 10 mA; V_{G2-S} = V_{DS} = 0	$\pm V_{(BR)G1-SS}$		6,0 to 20	V
$\pm I_{G2-SS}$ = 10 mA; V_{G1-S} = V_{DS} = 0	$\pm V_{(BR)G2-SS}$		6,0 to 20	V
Drain current (measured under pulse conditions)				
V_{DS} = 15 V; V_{G1-S} = 0; + V_{G2-S} = 4 V	I_{DSS}		4 to 20	mA
Gate-source cut-off voltages				
I_D = 20 μA; V_{DS} = 15 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	$<$	2,5	V
I_D = 20 μA; V_{DS} = 15 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	$<$	2,0	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source); I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$|y_{fs}|$	$>$	15	mS
		typ.	18	mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	2,5	pF
		$<$	3,0	pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1,2	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1,0	pF
Noise figure at G_S = 2 mS ; B_S = B_S opt f = 200 MHz	F	typ.	1,0	dB
Power gain at G_S = 2 mS ; B_S = B_S opt G_L = 0,5 mS; B_L = B_L opt; f = 200 MHz	G_p	typ.	25	dB

7Z80873

C_{ig1-s} (pF)

Fig. 3 $V_{G2-S} = 4$ V; $V_{DS} = 15$ V;
f = 1 MHz; $T_{amb} = 25$ °C; typical values.

7Z80875

C_{ig2-s} (pF)

Fig. 4 $V_{G1-S} = 0$ V; $V_{DS} = 15$ V;
f = 1 MHz; $T_{amb} = 25$ °C; typical values.

7Z80880

C_{os} (pF)

Fig. 5 $V_{G2-S} = 4$ V; $I_D = 10$ mA;
f = 1 MHz; $T_{amb} = 25$ °C; typical values.

7Z80879

$|y_{fs}|$ (mS)

Fig. 6 $V_{G2-S} = 4$; $V_{DS} = 15$ V;
f = 1 kHz; $T_{amb} = 25$ °C; typical values.

7Z80882

$|y_{fs}|$ (mS)

$|y_{fs}|$

$-\varphi_{fs}$

$-\varphi_{fs}$

Fig. 7 $V_{G2-S} = 4$ V; $V_{GS} = 15$ V;
$I_D = 10$ mA; $T_{amb} = 25$ °C; typical values.

7Z80877

g_{is} b_{is} (μS)

b_{is}

g_{is}

Fig. 8 $V_{G2-S} = 4$ V; $V_{DS} = 15$ V;
$I_D = 10$ mA; $T_{amb} = 25$ °C; typical values.

Fig. 9 V_{G2-S} = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 ^{o}C; typical values.

Fig. 10 V_{G2-S} = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 ^{o}C; typical values.

Fig. 11 V_{G2-S} = 4 V; V_{DS} = 15 V; I_D = 10 mA; f = 200 MHz; T_{amb} = 25 ^{o}C; typical values.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in plastic X-package with source and substrate interconnected, intended for v.h.f. applications, such as v.h.f. television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source and has an integrated drain resistance to suppress oscillation in the frequency range higher than 1 GHz.

This device is especially intended for use in pre-amplifiers in CATV tuners with large tuning ranges up to 500 MHz.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain-current	I_D	max.	30 mA
Total power dissipation up to $T_{amb} = 75\ ^oC$	P_{tot}	max.	225 mW
Transfer admittance at f = 1 kHz $I_D = 10$ mA; $V_{DS} = 15$ V; $V_{G2-S} = 4$ V	$|y_{fs}|$	typ.	18 mS
Feedback capacitance at f = 1 MHz $I_D = 10$ mA; $V_{DS} = 15$ V; $V_{G2-S} = 4$ V	C_{rs}	typ.	25 fF
Noise figure at $G_S = 2$ mS; $B_S = B_{Sopt}$ $I_D = 10$ mA; $V_{DS} = 15$ V; $V_{G2-S} = 4$ V; f = 200 MHz	F	typ.	1,0 dB

MECHANICAL DATA
Dimensions in mm

Fig. 1 SOT-103.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain-current (d.c. or average)	I_D	max.	30	mA
Gate 1-source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2-source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to $T_{amb} = 75\ ^oC$	P_{tot}	max.	225	mW
Storage temperature	T_{stg}	−65 to +150		^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to ambient in free air
  mounted on a printed-circuit board (see Fig. 2) $R_{th\ j\text{-}a}$ =   335 K/W

Dimensions in mm

(1) Connection made by a strip or Cu wire

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_{amb} = 25 °C unless stated otherwise

Gate cut-off currents

$\pm V_{G1\text{-}S}$ = 5 V; $V_{G2\text{-}S}$ = V_{DS} = 0	$\pm I_{G1\text{-}SS}$	<	50 nA
$\pm V_{G2\text{-}S}$ = 5 V; $V_{G1\text{-}S}$ = V_{DS} = 0	$\pm I_{G2\text{-}SS}$	<	50 nA

Gate-source breakdown voltages

$\pm I_{G1\text{-}SS}$ = 10 mA; $V_{G2\text{-}S}$ = V_{DS} = 0	$\pm V_{(BR)G1\text{-}SS}$		6,0 to 20 V
$\pm I_{G2\text{-}SS}$ = 10 mA; $V_{G1\text{-}S}$ = V_{DS} = 0	$\pm V_{(BR)G2\text{-}SS}$		6,0 to 20 V

Drain current

V_{DS} = 15 V; $V_{G1\text{-}S}$ = 0; $V_{G2\text{-}S}$ = 4 V; T_j = 25 °C	I_{DSS}		2,0 to 20 mA

Gate-source cut-off voltages

I_D = 20 μA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$-V_{(P)G1\text{-}S}$	<	2,5 V
I_D = 20 μA; V_{DS} = 15 V; + $V_{G1\text{-}S}$ = 0	$-V_{(P)G2\text{-}S}$	<	2,0 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source); I_D = 10 mA;
V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$|y_{fs}|$	>	15 mS
		typ.	18 mS
Input capacitance at gate 1 at f = 1 MHz	$C_{ig1\text{-}s}$	typ.	2,5 pF
Input capacitance at gate 2 at f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1,2 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1,0 pF
Noise figure at G_S = 2 mS; B_S = B_{Sopt} and f = 200 MHz	F	typ.	1,0 dB
Power gain at G_S = 2 mS; B_S = B_{Sopt} G_L = 0,5 mS; B_L = B_{Lopt}; f = 200 MHz	G_p	typ.	25 dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for u.h.f. applications in television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA
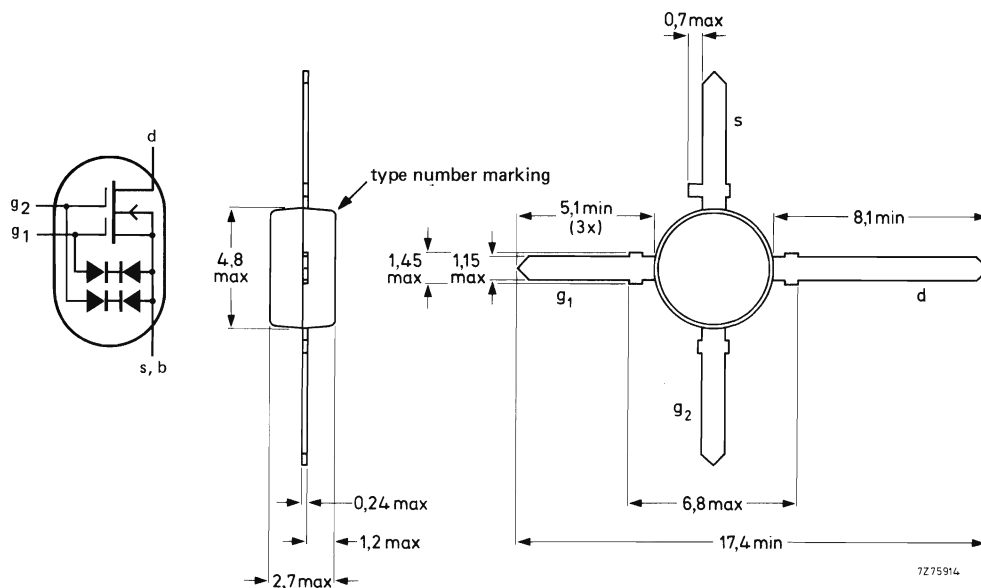
Drain-source voltage	V_{DS}	max.	20	V
Drain-current	I_D	max.	30	mA
Total power dissipation up to $T_{amb} = 75\ ^oC$	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	^oC
Transfer admittance at f = 1 kHz $I_D = 10$ mA; $V_{DS} = 15$ V; $+ V_{G2\text{-}S} = 4$ V	$|y_{fs}|$	typ.	17	mS
Feedback capacitance at f = 1 MHz $I_D = 10$ mA; $V_{DS} = 15$ V; $+ V_{G2\text{-}S} = 4$ V	C_{rs}	typ.	25	fF
Noise figure at $G_S = 2$ mS; $B_S = B_S$ opt $I_D = 10$ mA; $V_{DS} = 15$ V; $+ V_{G2\text{-}S} = 4$ V; f = 800 MHz	F	typ.	2,8	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

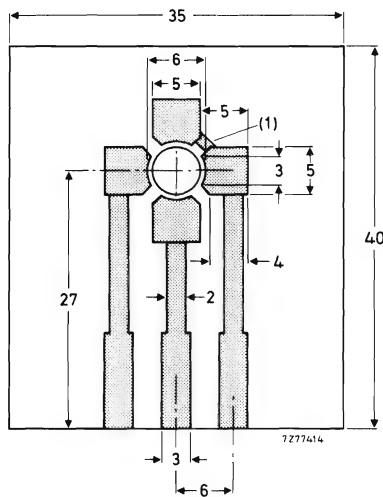|			
Drain source voltage	V_{DS}	max.	20 V
Drain current (d.c. or average)	I_D	max.	30 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 75\ ^oC$	P_{tot}	max.	225 mW
Storage temperature	T_{stg}		-65 to $+150\ ^oC$
Junction temperature	T_j	max.	150 ^oC

THERMAL RESISTANCE

From junction to ambient in free air
mounted on the printed-circuit board (see Fig. 2) $R_{th\,j-a}$ = 335 K/W

Dimensions in mm

(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

$T_{amb} = 25\ ^oC$

Gate cut-off currents				
$\pm V_{G1\text{-}S} = 5\ V;\ V_{G2\text{-}S} = V_{DS} = 0$	$\pm I_{G1\text{-}SS}$	$<$	50	nA
$\pm V_{G2\text{-}S} = 5\ V;\ V_{G1\text{-}S} = V_{DS} = 0$	$\pm I_{G2\text{-}SS}$	$<$	50	nA
Gate-source breakdown voltages				
$\pm I_{G1\text{-}SS} = 10\ mA;\ V_{G2\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G1\text{-}SS}$		6,0 to 20	V
$\pm I_{G2\text{-}SS} = 10\ mA;\ V_{G1\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G2\text{-}SS}$		6,0 to 20	V
Drain current*				
$V_{DS} = 15\ V;\ V_{G1\text{-}S} = 0;\ +V_{G2\text{-}S} = 4\ V$	I_{DSS}		2 to 20	mA
Gate-source cut-off voltages				
$I_D = 20\ \mu A;\ V_{DS} = 15\ V;\ +V_{G2\text{-}S} = 4\ V$	$-V_{(P)G1\text{-}S}$	$<$	2,5	V
$I_D = 20\ \mu A;\ V_{DS} = 15\ V;\ V_{G1\text{-}S} = 0$	$-V_{(P)G2\text{-}S}$	$<$	2,0	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10\ mA;\ V_{DS} = 15\ V;\ +V_{G2\text{-}S} = 4\ V;\ T_{amb} = 25\ ^oC$

Transfer admittance at f = 1 kHz	$|y_{fs}|$	$>$	15	mS
		typ.	17	mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	2,2	pF
		$<$	2,6	pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1,1	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25	fF
		$<$	35	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0,8	pF
		$<$	1,2	pF
Noise figure at $G_S = 2\ mS;\ B_S = B_S$ opt				
f = 200 MHz	F	typ.	1,5	dB
f = 800 MHz	F	typ.	2,8	dB
		$<$	3,9	dB
Power gain at $G_S = 2\ mS;\ B_S = B_S$ opt				
$G_L = 0,5\ mS;\ B_L = B_L$ opt; f = 200 MHz	G_p	typ.	25	dB
$G_L = 1\ mS;\ B_L = B_L$ opt; f = 800 MHz	G_p	typ.	18	dB

* Measured under pulse conditions.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for u.h.f. applications in television tuners and professional communication equipment.
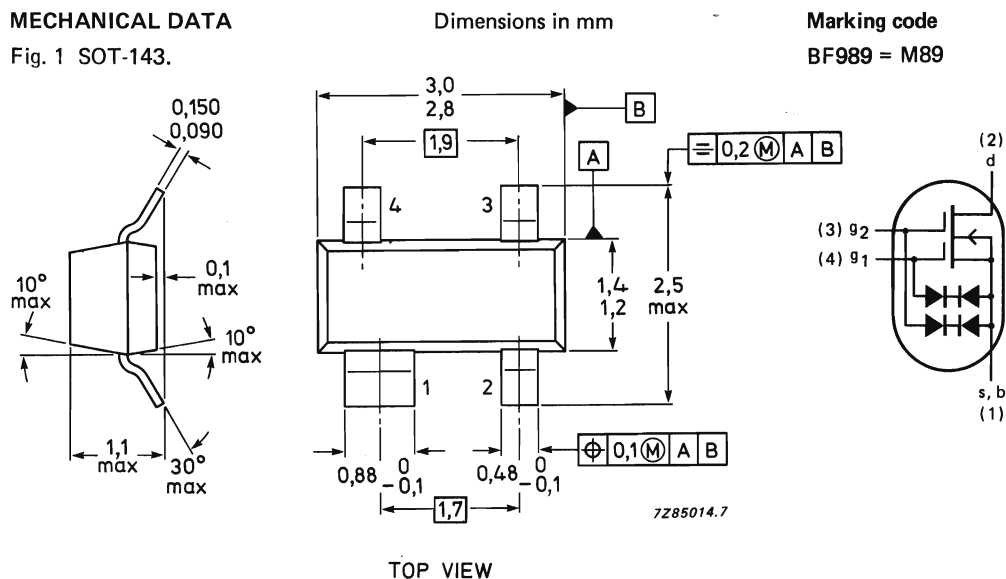
This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain-current	I_D	max.	30	mA
Total power dissipation up to $T_{amb} = 75\ ^oC$	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	^oC
Transfer admittance at $f = 1\,kHz$ $I_D = 10\,mA; V_{DS} = 15\,V; + V_{G2\text{-}S} = 4\,V$	$|y_{fs}|$	typ.	18	mS
Feedback capacitance at $f = 1\,MHz$ $I_D = 10\,mA; V_{DS} = 15\,V; + V_{G2\text{-}S} = 4\,V$	C_{rs}	typ.	25	fF
Noise figure at $G_S = 3,3\,mS; B_S = B_S$ opt $I_D = 10\,mA; V_{DS} = 15\,V; + V_{G2\text{-}S} = 4\,V; f = 800\,MHz$	F	typ.	1,8	dB

MECHANICAL DATA   Dimensions in mm

Fig. 1 SOT-103.

7Z75914A

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain-current (d.c. or average)	I_D	max.	30 mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 75\ ^oC$	P_{tot}	max.	225 mW
Storage temperature	T_{stg}		-65 to $+150\ ^oC$
Junction temperature	T_j	max.	150 ^oC

THERMAL RESISTANCE

From junction to ambient in free air
mounted on the printed-circuit board (see Fig. 2) $R_{th\ j\text{-}a}$ =   335 K/W

(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

$T_{amb} = 25\ ^oC$

Gate cut-off currents

$\pm V_{G1-S} = 5$ V; $V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	$<$	50 nA
$\pm V_{G2-S} = 5$ V; $V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	$<$	50 nA

Gate-source breakdown voltages

$\pm I_{G1-SS} = 10$ mA; $V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$		6,0 to 20 V
$\pm I_{G2-SS} = 10$ mA; $V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$		6,0 to 20 V

Drain current (measured under pulse conditions)

$V_{DS} = 15$ V; $V_{G1-S} = 0$; $+ V_{G2-S} = 4$ V	I_{DSS}		4 to 20 mA

Gate-source cut-off voltages

$I_D = 20\ \mu A$; $V_{DS} = 15$ V; $+ V_{G2-S} = 4$ V	$-V_{(P)G1-S}$	$<$	2,5 V
$I_D = 20\ \mu A$; $V_{DS} = 15$ V; $V_{G1-S} = 0$	$-V_{(P)G2-S}$	$<$	2,0 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10$ mA; $V_{DS} = 15$ V; $+ V_{G2-S} = 4$ V; $T_{amb} = 25\ ^oC$

Transfer admittance at f = 1 kHz	$|y_{fs}|$	$>$	15 mS
		typ.	18 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	2,3 pF
		$<$	2,6 pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1,1 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0,8 pF

Noise figure

f = 200 MHz; $G_S = 2$ mS; $B_S = B_S$ opt	F	-	typ.	1,0 dB ←
f = 800 MHz; $G_S = 3,3$ mS; $B_S = B_S$ opt	F		typ.	1,8 dB ←

Power gain

f = 200 MHz; $G_S = 2$ mS; $G_L = 0,5$ mS; $B_S =$ opt; $B_L =$ opt	G_p		typ.	25 dB ←
f = 800 MHz; $G_S = 3,3$ mS; $G_L = 1$ mS; $B_S =$ opt; $B_L =$ opt	G_p		typ.	18 dB ←
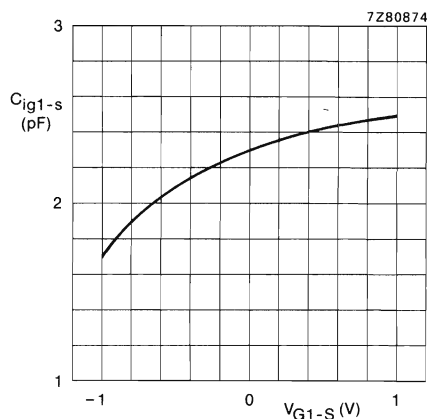
Fig. 3 $V_{G2-S} = 4$ V; $V_{DS} = 15$ V; f = 1 MHz; $T_{amb} = 25\ ^oC$; typical values.
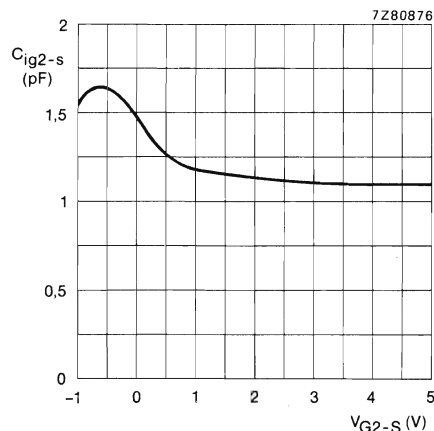
Fig. 4 $V_{G1-S} = 0$ V; $V_{DS} = 15$ V; f = 1 MHz; $T_{amb} = 25\ ^oC$; typical values.
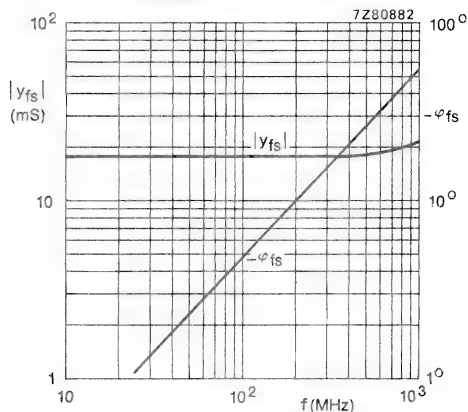
Fig. 5 V_{G2-S} = 4 V; I_D = 10 mA;
f = 1 MHz; T_{amb} = 25 °C; typical values.

Fig. 6 V_{G2-S} = 4 V; V_{DS} = 15 V;
f = 1 kHz; T_{amb} = 25 °C; typical values.
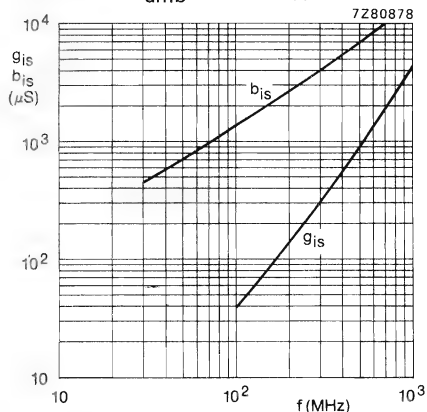
Fig. 7 V_{G2-S} = 4 V; V_{DS} = 15 V;
I_D = 10 mA; T_{amb} = 25 °C; typical values.

Fig. 8 V_{G2-S} = 4 V; V_{DS} = 15 V;
I_D = 10 mA; T_{amb} = 25 °C; typical values.
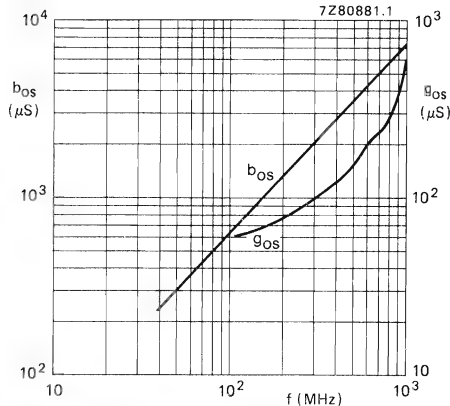
Fig. 9 V_{G2-S} = 4 V; V_{DS} = 15 V;
I_D = 10 mA; T_{amb} = 25 °C; typical values.

Fig. 10 V_{G2-S} = 4 V; V_{DS} = 15 V;
I_D = 10 mA; T_{amb} = 25 °C; typical values.

7Z94308
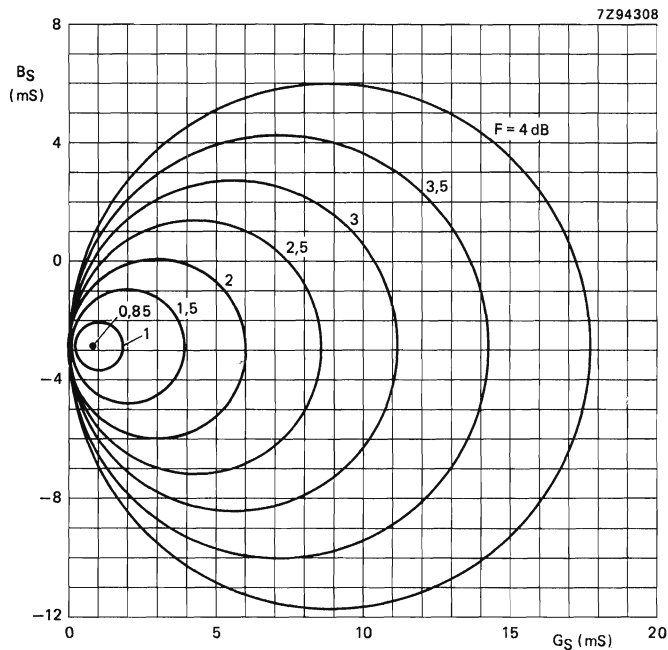
Fig. 11 V_{G2-S} = 4 V; V_{DS} = 15 V; I_D = 10 mA;
f = 200 MHz; T_{amb} = 25 °C; typical values.

7Z94309
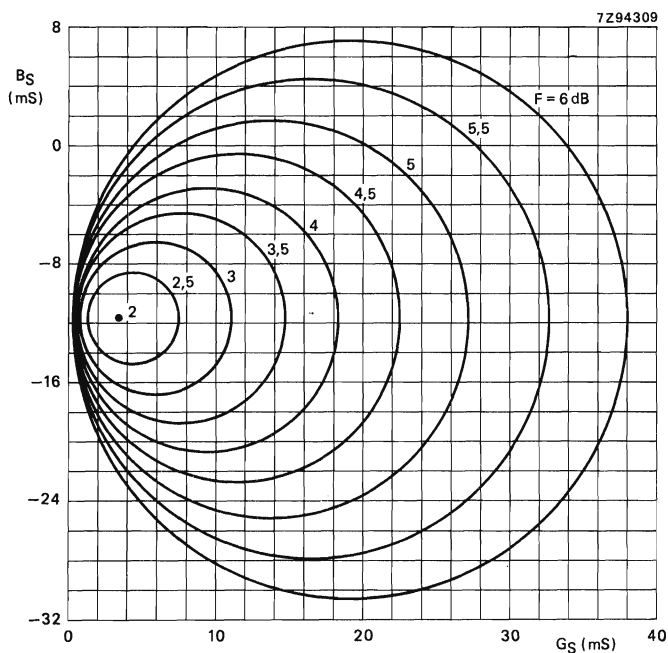
Fig. 12 V_{G2-S} = 4 V; V_{DS} = 15 V; I_D = 10 mA;
f = 800 MHz; T_{amb} = 25 °C; typical values.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for u.h.f. applications, such as u.h.f. television tuners, with 12 V supply voltage.

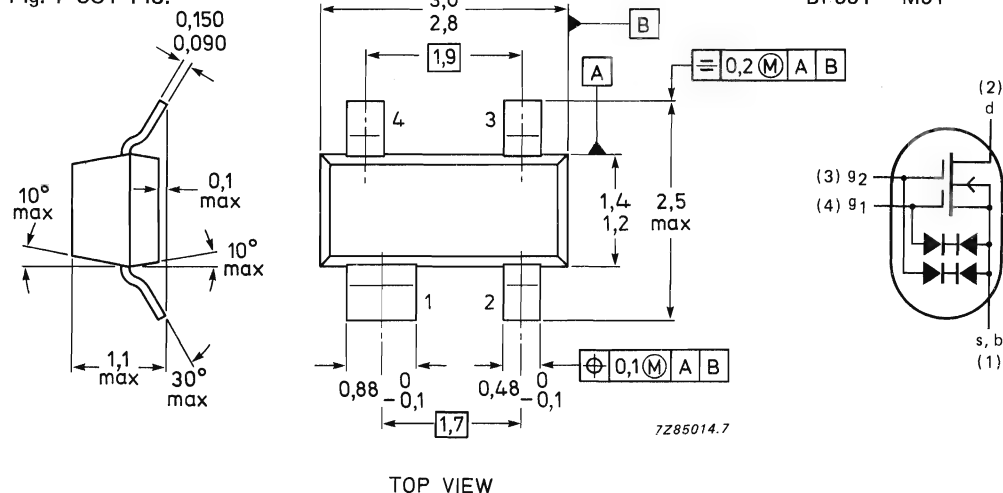This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	18	V
Drain current	I_D	max.	30	mA
Total power dissipation up to $T_{amb} = 75\ ^oC$	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	^oC
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; $+V_{G2-S}$ = 4 V	$|y_{fs}|$	typ.	19	mS
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; $+V_{G2-S}$ = 4 V	C_{rs}	typ.	25	fF
Noise figure at G_S = 5 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 10 V; $+V_{G2-S}$ = 4 V; f = 800 MHz	F	typ.	2,8	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.

BF980

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	18 V
Drain current (d.c. or average)	I_D	max.	30 mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 75\,^{o}C$	P_{tot}	max.	225 mW
Storage temperature	T_{stg}	-65 to $+150$	^{o}C
Junction temperature	T_j	max. 150	^{o}C

THERMAL RESISTANCE

From junction to ambient in free air
mounted on the printed-circuit board (see Fig. 2)　　$R_{th\,j\text{-}a}$ = 335 K/W

Dimensions in mm

(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

$T_{amb} = 25\ ^oC$

Gate cut-off currents

$\pm\ V_{G1-S} = 7$ V; $V_{G2-S} = V_{DS} = 0$	$\pm\ I_{G1-SS}$	$<$	25 nA
$\pm\ V_{G2-S} = 7$ V; $V_{G1-S} = V_{DS} = 0$	$\pm\ I_{G2-SS}$	$<$	25 nA

Gate-source breakdown voltages

$\pm\ I_{G1-SS} = 10$ mA; $V_{G2-S} = V_{DS} = 0$	$\pm\ V_{(BR)G1-SS}$	$>$	8 V
$\pm\ I_{G2-SS} = 10$ mA; $V_{G1-S} = V_{DS} = 0$	$\pm\ V_{(BR)G2-SS}$	$>$	8 V

Gate-source cut-off voltages

$I_D = 20\ \mu A$; $V_{DS} = 10$ V; $+\ V_{G2-S} = 4$ V	$-V_{(P)G1-S}$	$<$	1,3 V
		$>$	0,2 V
$I_D = 20\ \mu A$; $V_{DS} = 10$ V; $V_{G1-S} = 0$	$-V_{(P)G2-S}$	$<$	1,1 V
		$>$	0,2 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10$ mA; $V_{DS} = 10$ V; $+\ V_{G2-S} = 4$ V; $T_{amb} = 25\ ^oC$

Transfer admittance at f = 1 kHz	$|y_{fs}|$	$>$	17 mS
		typ.	19 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	$<$	3,0 pF
		typ.	2,6 pF
Feedback capacitance at f = 1 MHz	C_{rs}	$<$	35 fF
		typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	$<$	1,3 pF
		typ.	1,1 pF
Noise figure at f = 800 MHz; $G_S = 5$ mS; $B_S = B_S$ opt	F	$<$	3,9 dB
		typ.	2,8 dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for v.h.f. applications, such as v.h.f. television tuners, f.m. tuners and professional communication equipment.
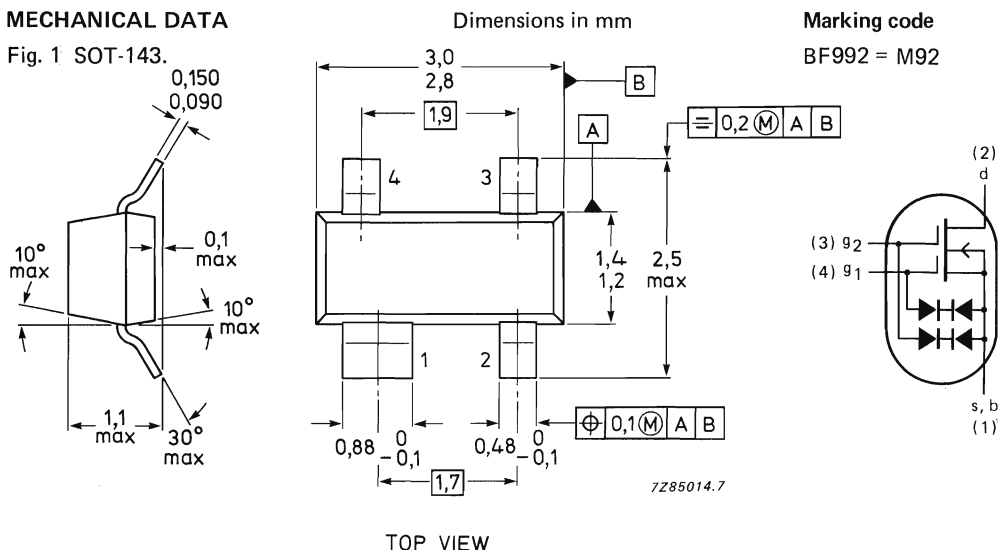
This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	20	mA
Total power dissipation up to $T_{amb} = 75$ °C	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz $I_D = 10$ mA; $V_{DS} = 10$ V; $+V_{G2-S} = 4$ V	$\|Y_{fs}\|$	typ.	14	mS
Feedback capacitance at f = 1 MHz $I_D = 10$ mA; $V_{DS} = 10$ V; $+V_{G2-S} = 4$ V	C_{rs}	typ.	20	fF
Noise figure at optimum source admittance $I_D = 10$ mA; $V_{DS} = 10$ V; $+V_{G2-S} = 4$ V; f = 200 MHz	F	typ.	0,7	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.

7Z75914

BF981

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (d.c. or average)	I_D	max.	20	mA
Drain current (peak value)	I_{DM}	max.	30	mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 75 ^{o}C	P_{tot}	max.	225	mW
Storage temperature	T_{stg}		−65 to + 150	^{o}C
Junction temperature	T_j	max.	150	^{o}C

THERMAL RESISTANCE

From junction to ambient in free air
  mounted on the printed-circuit board (see Fig. 2) $\quad R_{th\,j\text{-}a} \quad = \quad 335$ K/W

Dimensions in mm

(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

$T_{amb} = 25\ ^oC$ unless otherwise specified

Gate cut-off currents

$\pm V_{G1-S} = 5\ V;\ V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	$<$	50 nA
$\pm V_{G2-S} = 5\ V;\ V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	$<$	50 nA

Gate-source breakdown voltages

$\pm I_{G1-SS} = 10\ mA;\ V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$	$>$	6 V
$\pm I_{G2-SS} = 10\ mA;\ V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$	$>$	6 V

Drain current

$V_{DS} = 10\ V;\ V_{G1-S} = 0;\ + V_{G2-S} = 4\ V;\ T_j = 25\ ^oC$	I_{DSS}	4 to 25 mA

Gate-source cut-off voltages

$I_D = 20\ \mu A;\ V_{DS} = 10\ V;\ + V_{G2-S} = 4\ V$	$-V_{(P)G1-S}$	$<$	2,5 V
$I_D = 20\ \mu A;\ V_{DS} = 10\ V;\ V_{G1-S} = 0$	$-V_{(P)G2-S}$	$<$	2,5 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10\ mA;\ V_{DS} = 10\ V;\ + V_{G2-S} = 4\ V;\ T_{amb} = 25\ ^oC$

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	$>$ typ.	10 mS 14 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	2,1 pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1,0 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	20 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1,1 pF
Noise figure at f = 100 MHz; G_S = 1 mS; B_S = B_S opt	F	typ. $<$	0,7 dB 1,7 dB
Noise figure at f = 200 MHz; G_S = 2 mS; B_S = B_S opt	F	typ. $<$	1,0 dB 2,0 dB
Transducer gain at f = 100 MHz; G_S = 1 mS; B_S = B_S opt; G_L = 0,5 mS; B_L = B_L opt	G_{tr}	typ.	29 dB
Transducer gain at f = 200 MHz; G_S = 2 mS; B_S = B_S opt; G_L = 0,5 mS; B_L = B_L opt	G_{tr}	typ.	26 dB

7Z82223
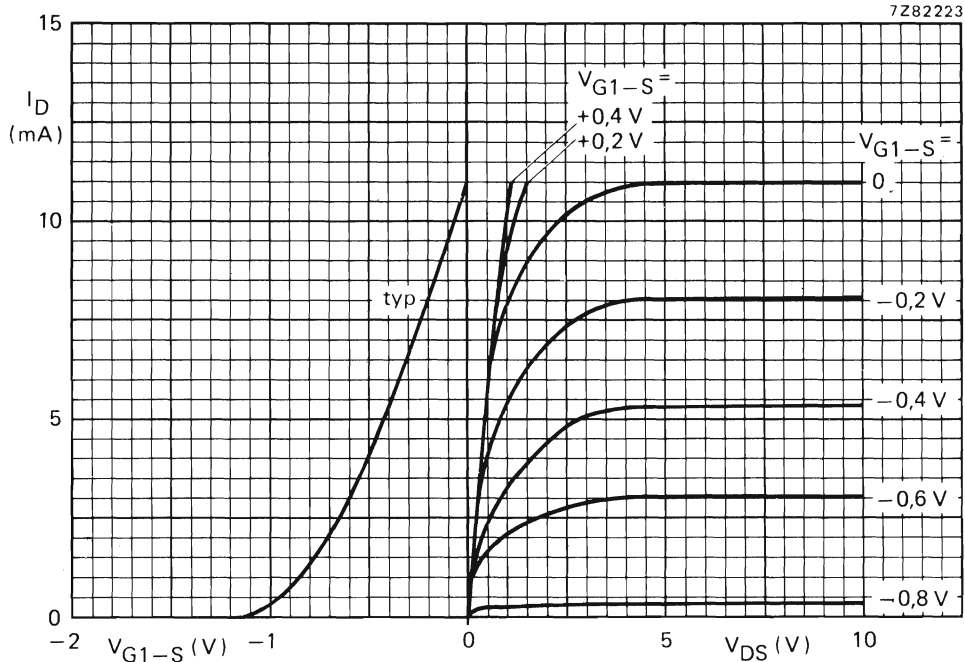
Fig. 3 **Left-hand graph:** $V_{DS} = 10$ V; $V_{G2-S} = +4$ V; $T_{amb} = 25$ °C. **Right-hand graph:** $V_{G2-S} = +4$ V; $T_{amb} = 25$ °C.
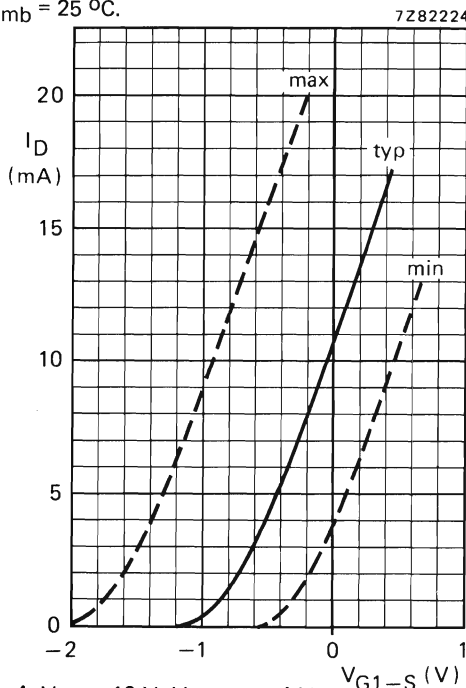
Fig. 4 $V_{DS} = 10$ V; $V_{G2-S} = +4$ V; $T_{amb} = 25$ °C.
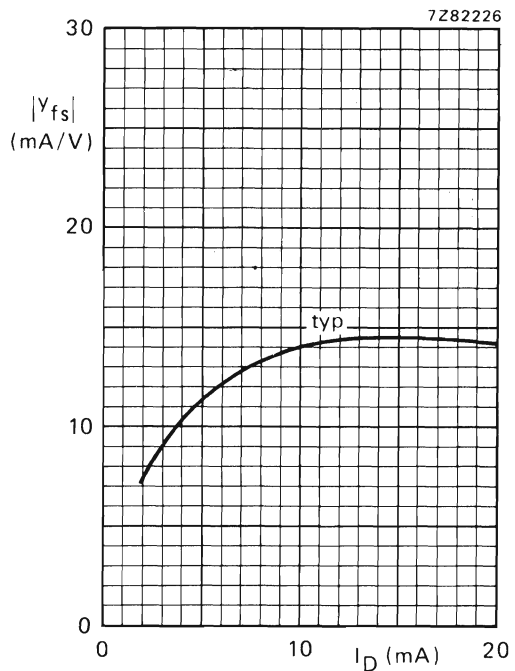
Fig. 5 $V_{DS} = 10$ V; $V_{G2-S} = +4$ V; $f = 1$ kHz; $T_{amb} = 25$ °C.

7Z82692

Fig. 6.

7Z82691

Fig. 7.

7Z82690
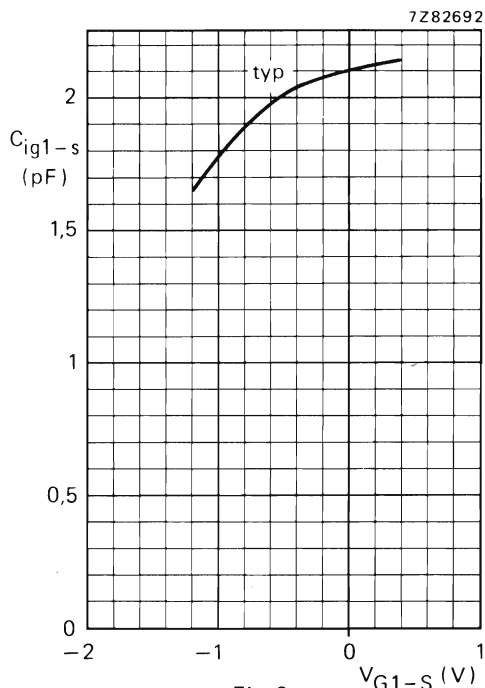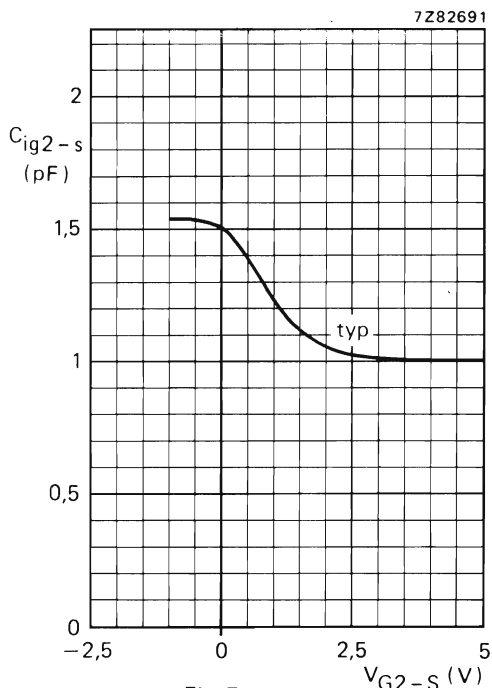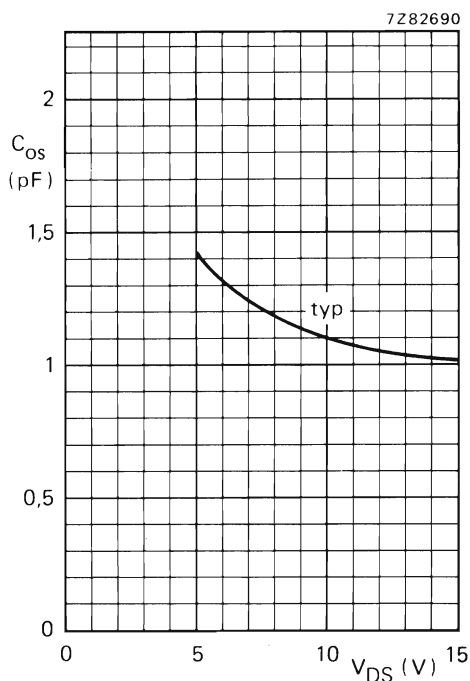
Fig. 8.

Measuring conditions:

Fig. 6 V_{DS} = 10 V; $V_{G2\text{-}S}$ = + 4 V; f = 1 MHz; T_{amb} = 25 °C.

Fig. 7 V_{DS} = 10 V; $V_{G1\text{-}S}$ = 0; f = 1 MHz; T_{amb} = 25 °C.

Fig. 8 $V_{G2\text{-}S}$ = + 4 V; I_D = 10 mA; f = 1 MHz; T_{amb} = 25 °C.

Measuring conditions for Figs 9 to 12: V_{DS} = 10 V; I_D = 10 mA; $V_{G2\text{-}S}$ = + 4 V; T_{amb} = 25 °C.
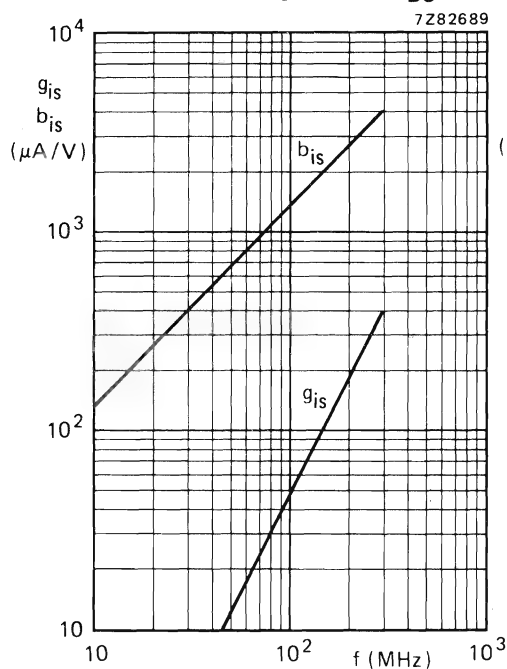
Fig. 9.
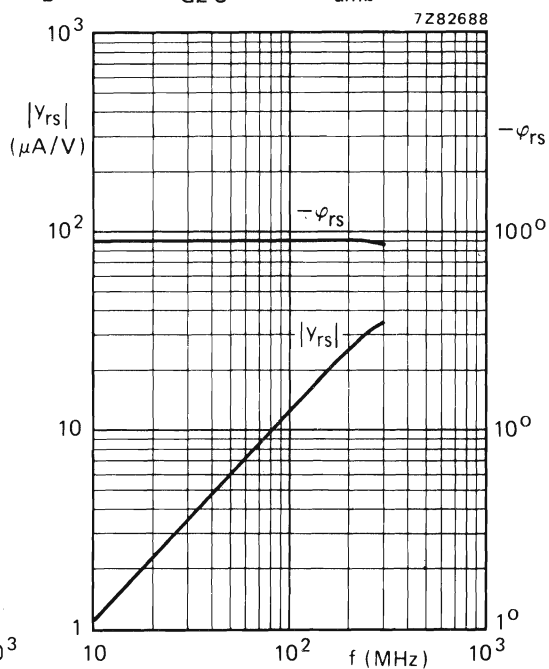
Fig. 10.
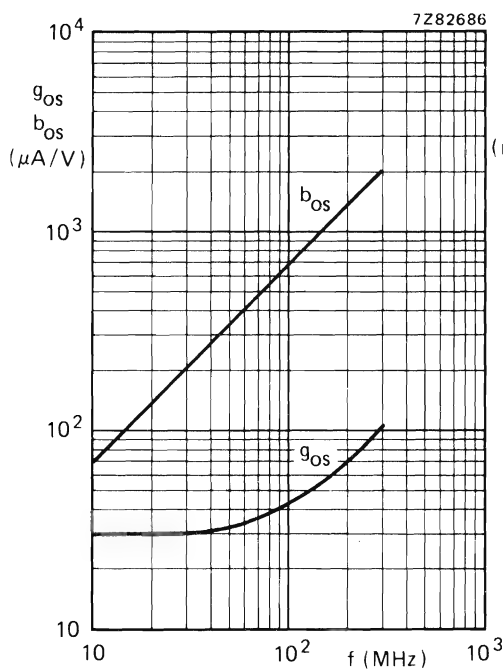
Fig. 11.
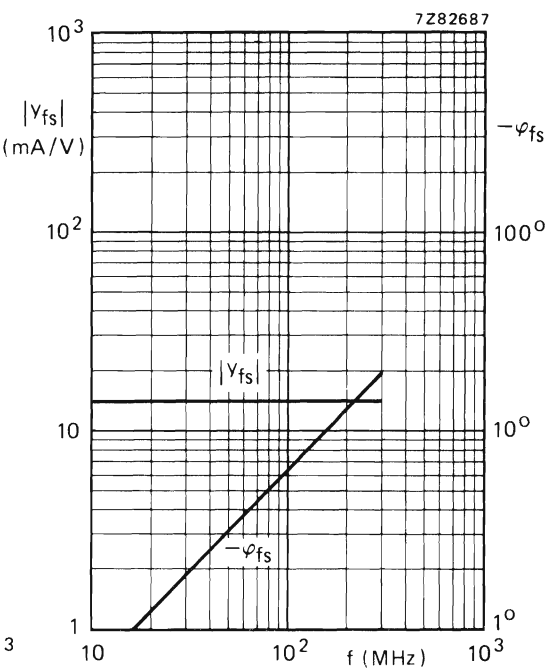
Fig. 12.
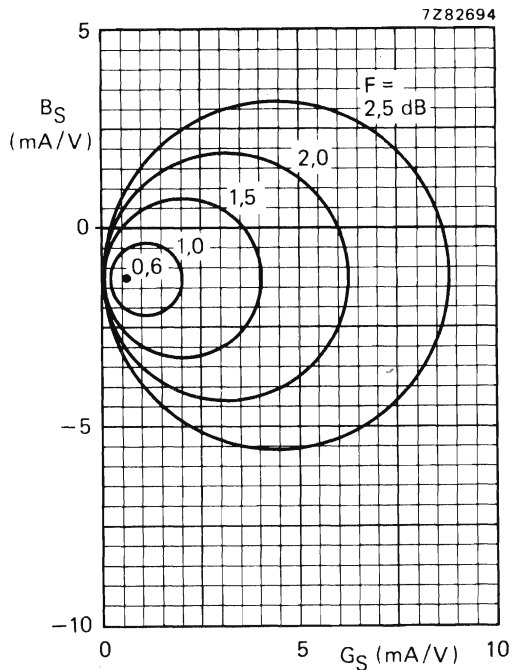
Fig. 13 V_{DS} = 10 V; V_{G2-S} = + 4 V; I_D = 10 mA;
f = 100 MHz; T_{amb} = 25 °C; circles of typical
constant noise figures.
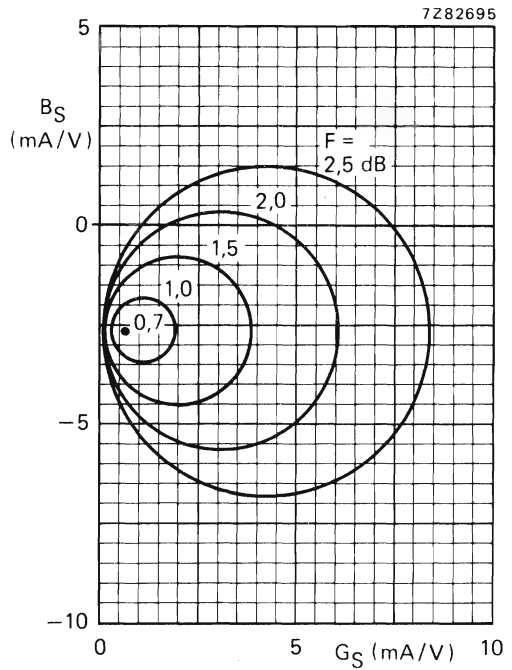
Fig. 14 V_{DS} = 10 V; V_{G2-S} = + 4 V; I_D = 10 mA;
f = 200 MHz; T_{amb} = 25 °C; circles of typical
constant noise figures.
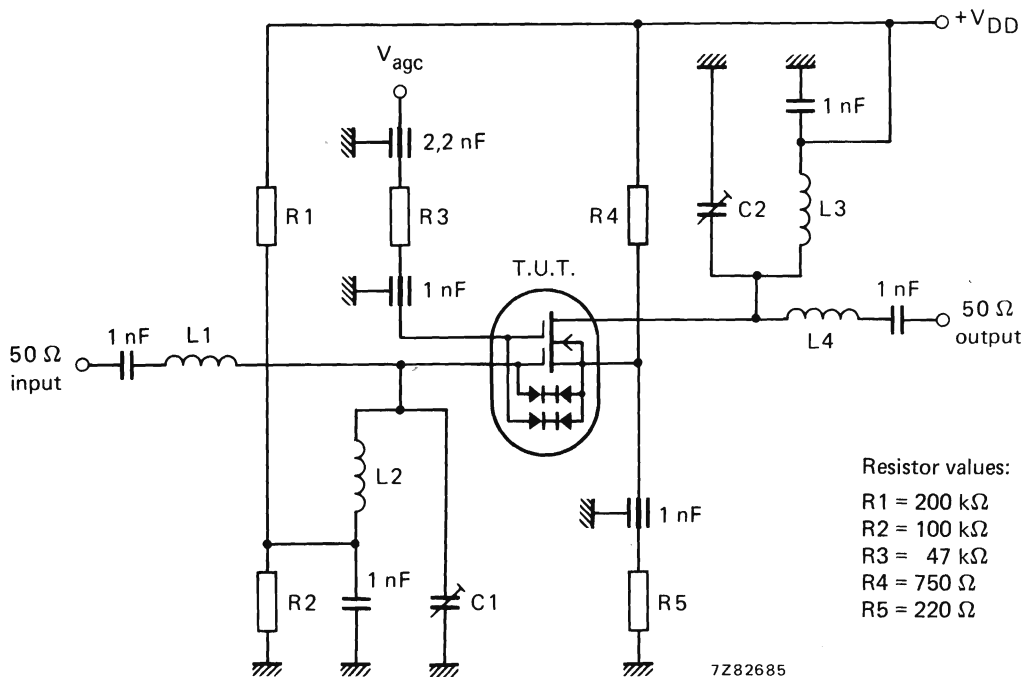
Fig. 15 Automatic gain control test circuit at f = 200 MHz (see also Fig. 16).
V_{DD} = 16 V; G_S = 2 mA/V; G_L = 0,5 mA/V.

Resistor values:

$R1 = 200\ k\Omega$
$R2 = 100\ k\Omega$
$R3 = 47\ k\Omega$
$R4 = 750\ \Omega$
$R5 = 220\ \Omega$
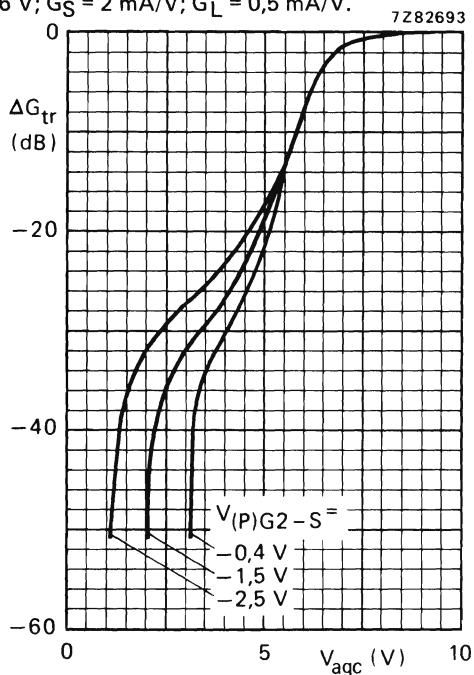
Fig. 16 V_{DD} = 16 V; f = 200 MHz;
T_{amb} = 25 °C; typical values;
see also Fig. 15.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for v.h.f. applications, such as v.h.f. television tuners, f.m. tuners, with 12 V supply voltage.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	40	mA
Total power dissipation up to $T_{amb} = 75\,^{\circ}C$	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	$^{\circ}C$
Transfer admittance at f = 1 kHz $I_D = 15$ mA; $V_{DS} = 10$ V; $+V_{G2-S} = 4$ V	$|y_{fs}|$	typ.	25	mS
Feedback capacitance at f = 1 MHz $I_D = 15$ mA; $V_{DS} = 10$ V; $+V_{G2-S} = 4$ V	C_{rs}	typ.	30	fF
Noise figure at $G_S = 2$ mS; $B_S = B_S$ opt $I_D = 15$ mA; $V_{DS} = 10$ V; $+V_{G2-S} = 4$ V; f = 200 MHz	F	typ.	1,2	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (d.c. or average)	I_D	max.	40	mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10	mA
Total power dissipation up to $T_{amb} = 75\ ^oC$	P_{tot}	max.	225	mW
Storage temperature	T_{stg}	-65 to $+150$		^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to ambient in free air
mounted on the printed-circuit board (see Fig. 2) $R_{th\ j-a}$ = 335 K/W

Dimensions in mm

(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

$T_{amb} = 25 \, ^oC$

Gate cut-off currents

$\pm V_{G1\text{-}S} = 7 \, V; V_{G2\text{-}S} = V_{DS} = 0$	$\pm I_{G1\text{-}SS}$	$<$	25	nA
$\pm V_{G2\text{-}S} = 7 \, V; V_{G1\text{-}S} = V_{DS} = 0$	$\pm I_{G2\text{-}SS}$	$<$	25	nA

Gate-source breakdown voltages

$\pm I_{G1\text{-}SS} = 10 \, mA; V_{G2\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G1\text{-}SS}$	$>$	8	V
$\pm I_{G2\text{-}SS} = 10 \, mA; V_{G1\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G2\text{-}SS}$	$>$	8	V

Gate-source cut-off voltages

$I_D = 20 \, \mu A; V_{DS} = 10 \, V; +V_{G2\text{-}S} = 4 \, V$	$-V_{(P)G1\text{-}S}$	$<$	1,3	V
$I_D = 20 \, \mu A; V_{DS} = 10 \, V; V_{G1\text{-}S} = 0$	$-V_{(P)G2\text{-}S}$	$<$	1,1	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 15 \, mA; V_{DS} = 10 \, V; + V_{G2\text{-}S} = 4 \, V; T_{amb} = 25 \, ^oC$

Transfer admittance at f = 1 kHz	$\|y_{fs}\|$	$>$	20	mS
		typ.	25	mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	4,0	pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1,7	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	30	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	2,0	pF
Noise figure at f = 200 MHz; $G_S = 2 \, mS; B_S = B_S$ opt	F	typ.	1,2	dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT-143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in u.h.f. applications in television tuners. The device is also suitable for use in professional communication equipment.
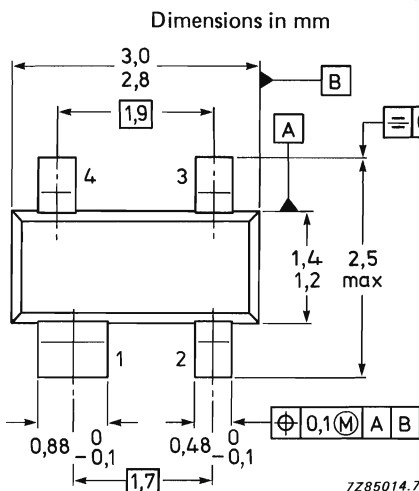
The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current (peak value)	I_{DM}	max.	30	mA
Total power dissipation up to $T_{amb} = 60\ ^{\circ}C$	P_{tot}	max.	200	mW
Junction temperature	T_j	max.	150	$^{\circ}C$
Transfer admittance at $f = 1\ kHz$ $I_D = 7\ mA; V_{DS} = 10\ V; + V_{G2\text{-}S} = 4\ V$	$|y_{fs}|$	typ.	12	mS
Feedback capacitance at $f = 1\ MHz$ $I_D = 7\ mA; V_{DS} = 10\ V; + V_{G2\text{-}S} = 4\ V$	C_{rs}	typ.	25	fF
Noise figure at $G_S = 2\ mS; B_S = B_S$ opt $I_D = 7\ mA; V_{DS} = 10\ V; + V_{G2\text{-}S} = 4\ V; f = 800\ MHz$	F	typ.	2,8	dB

MECHANICAL DATA

Fig. 1 SOT-143.

Dimensions in mm

Marking code

BF989 = M89

TOP VIEW

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (d.c. or average)	I_D	max.	20	mA
Drain current (peak value)	I_{DM}	max.	30	mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to $T_{amb} = 60\,^oC^*$	P_{tot}	max.	200	mW
Storage temperature	T_{stg}		-65 to $+150$	^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j\text{-}a}$	$=$	460	K/W

STATIC CHARACTERISTICS

$T_{amb} = 25\,^oC$ unless otherwise specified

Gate cut-off currents				
$\pm V_{G1\text{-}S} = 5$ V; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm I_{G1\text{-}SS}$	$<$	50	nA
$\pm V_{G2\text{-}S} = 5$ V; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm I_{G2\text{-}SS}$	$<$	50	nA
Drain current				
$V_{DS} = 10$ V; $V_{G1\text{-}S} = 0$; $+ V_{G2\text{-}S} = 4$ V; $T_j = 25\,^oC$	I_{DSS}		2 to 20	mA
Gate-source breakdown voltages				
$\pm I_{G1\text{-}SS} = 10$ mA; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G1\text{-}SS}$		6 to 20	V
$\pm I_{G2\text{-}SS} = 10$ mA; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G2\text{-}SS}$		6 to 20	V
Gate-source cut-off voltages				
$I_D = 20\ \mu A$; $V_{DS} = 10$ V; $+ V_{G2\text{-}S} = 4$ V	$-V_{(P)G1\text{-}S}$	$<$	2,7	V
$I_D = 20\ \mu A$; $V_{DS} = 10$ V; $V_{G1\text{-}S} = 0$	$-V_{(P)G2\text{-}S}$	$<$	2,7	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 7$ mA; $V_{DS} = 10$ V; $+ V_{G2\text{-}S} = 4$ V; $T_{amb} = 25\,^oC$

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	$>$	9,5	mS
		typ.	12	mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	1,8	pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1,0	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0,9	pF
Noise figure at $G_S = 2$ mS; $B_S = B_S$ opt				
f = 200 MHz	F	typ.	1,6	dB
f = 800 MHz	F	typ.	2,8	dB

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic microminiature envelope with source and substrate interconnected, intended for u.h.f. applications, such as u.h.f. television tuners and professional communication equipment.
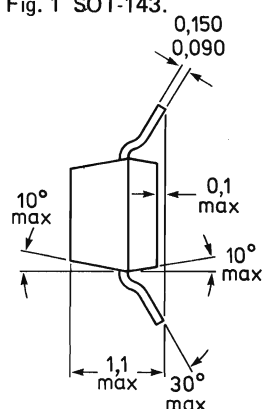
This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	18	V
Drain current (average)	$I_{D(AV)}$	max.	30	mA
Total power dissipation up to $T_{amb} = 60\ ^oC$	P_{tot}	max.	200	mW
Junction temperature	T_j	max.	150	^oC
Transfer admittance at $f = 1\ kHz$ $I_D = 10\ mA; V_{DS} = 10\ V; + V_{G2-S} = 4\ V$	$|y_{fs}|$	typ.	19	mS
Feedback capacitance at $f = 1\ MHz$ $I_D = 10\ mA; V_{DS} = 10\ V; + V_{G2-S} = 4\ V$	C_{rs}	typ.	25	fF
Noise figure at optimum source admittance $I_D = 10\ mA; V_{DS} = 10\ V; + V_{G2-S} = 4\ V; f = 800\ MHz$	F	typ.	2,8	dB

MECHANICAL DATA

Dimensions in mm

Marking code

Fig. 1 SOT-143.

BF990 = M90

TOP VIEW

7Z85014.7

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	18	V
Drain current (average)	$I_{D(AV)}$	max.	30	mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10	mA
Total power dissipation up to $T_{amb} = 60\ ^{o}C$*	P_{tot}	max.	200	mW
Storage temperature	T_{stg}		-65 to $+150$	^{o}C
Junction temperature	T_j	max.	150	^{o}C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\,j\text{-}a}$	=	460	K/W

Fig. 2 Power derating curve.

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

STATIC CHARACTERISTICS

$T_{amb} = 25\ ^oC$ unless otherwise specified

Gate cut-off currents

gate 1; $\pm V_{G1-S} = 7\ V;\ V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	<	25 nA
gate 2; $\pm V_{G2-S} = 7\ V;\ V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	<	25 nA

Gate-source breakdown voltages

gate 1; $\pm I_{G1-SS} = 10\ mA;\ V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$	>	8 V
gate 2; $\pm I_{G2-SS} = 10\ mA;\ V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$	>	8 V

Gate-source cut-off voltages

gate 1; $I_D = 20\ \mu A;\ V_{DS} = 10\ V;\ + V_{G2-S} = 4\ V$	$-V_{(P)G1-S}$	<	1,3 V
gate 2; $I_D = 20\ \mu A;\ V_{DS} = 10\ V;\ V_{G1-S} = 0$	$-V_{(P)G2-S}$	<	1,1 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10\ mA;\ V_{DS} = 10\ V;\ + V_{G2-S} = 4\ V;\ T_{amb} = 25\ ^oC$

Transfer admittance at f = 1 kHz	$|y_{fs}|$	>	17 mS
		typ.	19 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	2,6 pF
		<	3,0 pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1,4 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1,2 pF
Noise figure at f = 800 MHz; $G_S = 5\ mS$; $B_S = B_S$ opt	F	typ.	2,8 dB ⟵

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT-143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in v.h.f. applications, such as v.h.f. television tuners and f.m. tuners. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	20	mA
Total power dissipation up to $T_{amb} = 60\ ^oC$	P_{tot}	max.	200	mW
Junction temperature	T_j	max.	150	^oC
Transfer admittance at f = 1 kHz $I_D = 10$ mA; $V_{DS} = 10$ V; $+ V_{G2-S} = 4$ V	$\lvert y_{fs}\rvert$	typ.	14	mS
Feedback capacitance at f = 1 MHz $I_D = 10$ mA; $V_{DS} = 10$ V; $+ V_{G2-S} = 4$ V	C_{rs}	typ.	20	fF
Noise figure at optimum source admittance $I_D = 10$ mA; $V_{DS} = 10$ V; $+ V_{G2-S} = 4$ V; f = 200 MHz	F	typ.	0,7	dB

MECHANICAL DATA

Dimensions in mm

Marking code

Fig. 1 SOT-143.

BF991 = M91

TOP VIEW

See also *Soldering recommendations*.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (d.c. or average)	I_D	max.	20	mA
Drain current (peak value)	I_{DM}	max.	30	mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10	mA
Total power dissipation up to T_{amb} = 60 ^oC*	P_{tot}	max.	200	mW
Storage temperature	T_{stg}		-65 to $+150$	^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\,j-a}$	=	460	K/W

STATIC CHARACTERISTICS

T_{amb} = 25 ^oC unless otherwise specified

Gate cut-off currents				
$\pm V_{G1-S}$ = 5 V; $V_{G2-S} = V_{DS}$ = 0	$\pm I_{G1-SS}$	$<$	50	nA
$\pm V_{G2-S}$ = 5 V; $V_{G1-S} = V_{DS}$ = 0	$\pm I_{G2-SS}$	$<$	50	nA
Drain current				
V_{DS} = 10 V; V_{G1-S} = 0; $+ V_{G2-S}$ = 4 V; T_j = 25 ^oC	I_{DSS}		4 to 25	mA
Gate-source breakdown voltages				
$\pm I_{G1-SS}$ = 10 mA; $V_{G2-S} = V_{DS}$ = 0	$\pm V_{(BR)G1-SS}$	$>$	6	V
$\pm I_{G2-SS}$ = 10 mA; $V_{G1-S} = V_{DS}$ = 0	$\pm V_{(BR)G2-SS}$	$>$	6	V
Gate-source cut-off voltages				
I_D = 20 μA; V_{DS} = 10 V; $+ V_{G2-S}$ = 4 V	$-V_{(P)G1-S}$	$<$	2,5	V
I_D = 20 μA; V_{DS} = 10 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	$<$	2,5	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 10 V; $+ V_{G2-S}$ = 4 V; T_{amb} = 25 ^oC

Transfer admittance at f = 1 kHz	$|y_{fs}|$	$>$	10	mS
		typ.	14	mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	2,1	pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1,0	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	20	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1,1	pF
Noise figure				
→ f = 100 MHz; G_S = 1 mS; $B_S = B_S$ opt	F	typ.	0,7	dB
		$<$	1,7	dB
→ f = 200 MHz; G_S = 2 mS; $B_S = B_S$ opt	F	typ.	1,0	dB
		$<$	2,0	dB
Transducer gain **				
→ f = 100 MHz; G_S = 1 mS; $B_S = B_S$ opt; G_L = 0,5 mS; $B_L = B_L$ opt	G_{tr}	typ.	29	dB
→ f = 200 MHz; G_S = 2 mS; $B_S = B_S$ opt; G_L = 0,5 mS; $B_L = B_L$ opt	G_{tr}	typ.	26	dB

*   Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

**   Crystal mounted in a SOT-103 envelope.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT-143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in v.h.f. applications, such as v.h.f. television tuners, FM tuners with a 12 volt supply voltage. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	40	mA
Total power dissipation up to $T_{amb} = 60\ ^{\circ}C$	P_{tot}	max.	200	mW
Junction temperature	T_j	max.	150	$^{\circ}C$
Transfer admittance at f = 1 kHz				
$I_D = 15$ mA; $V_{DS} = 10$ V; $+ V_{G2-S} = 4$ V	$|Y_{fs}|$	typ.	25	mS
Feedback capacitance at f = 1 MHz				
$I_D = 15$ mA; $V_{DS} = 10$ V; $+ V_{G2-S} = 4$ V	C_{rs}	typ.	30	fF
Noise figure at $G_S = 2$ mS				
$I_D = 15$ mA; $V_{DS} = 10$ V; $+ V_{G2-S} = 4$ V; f = 200 MHz	F	typ.	1,2	dB

MECHANICAL DATA

Dimensions in mm

Marking code

Fig. 1 SOT-143.

BF992 = M92

TOP VIEW

See also *Soldering recommendations*.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (d.c. or average)	I_D	max.	40	mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10	mA
Total power dissipation up to $T_{amb} = 60\ ^oC*$	P_{tot}	max.	200	mW
Storage temperature	T_{stg}		-65 to $+150$	^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j-a}$	=	460	K/W

STATIC CHARACTERISTICS

$T_{amb} = 25\ ^oC$ unless otherwise specified

Gate cut-off currents

$\pm V_{G1-S} = 7$ V; $V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	$<$	25	nA
$\pm V_{G2-S} = 7$ V; $V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	$<$	25	nA

Gate-source breakdown voltages

$\pm I_{G1-SS} = 10$ mA; $V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$	$>$	8	V
$\pm I_{G2-SS} = 10$ mA; $V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$	$>$	8	V

Gate-source cut-off voltages

$I_D = 20\ \mu A$; $V_{DS} = 10$ V; $+ V_{G2-S} = 4$ V	$-V_{(P)G1-S}$	0,2 to 1,3	V
$I_D = 20\ \mu A$; $V_{DS} = 10$ V; $V_{G1-S} = 0$	$-V_{(P)G2-S}$	0,2 to 1,1	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 15$ mA; $V_{DS} = 10$ V; $+ V_{G2-S} = 4$ V; $T_{amb} = 25\ ^oC$

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	$>$	20	mS
		typ.	25	mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	4	pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1,7	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	30	fF
		$<$	40	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	2	pF
Noise figure at f = 200 MHz; $G_S = 2$ mS	F	typ.	1,2	dB

→ * Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic microminiature envelope with source and substrate interconnected, intended for u.h.f. and v.h.f. applications, such as u.h.f./v.h.f. television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current (average)	$I_{D(AV)}$	max.	30	mA
Total power dissipation up to $T_{amb} = 60\ ^oC$	P_{tot}	max.	200	mW
Junction temperature	T_j	max.	150	^oC
Transfer admittance at f = 1 kHz $I_D = 10$ mA; $V_{DS} = 15$ V; $+ V_{G2-S} = 4$ V	$|y_{fs}|$	typ.	17	mS
Feedback capacitance at f = 1 MHz $I_D = 10$ mA; $V_{DS} = 15$ V; $+ V_{G2-S} = 4$ V	C_{rs}	typ.	25	fF
Noise figure at optimum source admittance $I_D = 10$ mA; $V_{DS} = 15$ V; $+ V_{G2-S} = 4$ V; f = 200 MHz	F	typ.	1,5	dB

MECHANICAL DATA

Dimensions in mm

Marking code

Fig. 1 SOT-143.

BF994 = M94

TOP VIEW

See also *Soldering recommendations.*

BF994

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (average)	$I_{D(AV)}$	max.	30 mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 60\ ^oC^*$	P_{tot}	max.	200 mW
Storage temperature	T_{stg}		−65 to + 150 ^oC
Junction temperature	T_j	max.	150 ^oC

THERMAL RESISTANCE

From junction to ambient in free air* $R_{th\,j-a}$ = 460 K/W

Fig. 2 Power derating curve.

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,6 mm.

STATIC CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Gate cut-off currents

    gate 1;

$\pm V_{G1-S}$ = 5 V; $V_{G2-S} = V_{DS}$ = 0	$\pm I_{G1-SS}$	$<$	50 nA

    gate 2;

$\pm V_{G2-S}$ = 5 V; $V_{G1-S} = V_{DS}$ = 0	$\pm I_{G2-SS}$	$<$	50 nA

Gate-source breakdown voltages

    gate 1;

$\pm I_{G1-SS}$ = 10 mA; $V_{G2-S} = V_{DS}$ = 0	$\pm V_{(BR)G1-SS}$	6 to 20 V

    gate 2;

$\pm I_{G2-SS}$ = 10 mA; $V_{G1-S} = V_{DS}$ = 0	$\pm V_{(BR)G2-SS}$	6 to 20 V

Gate-source cut-off voltages

    gate 1;

I_D = 20 μA; V_{DS} = 15 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	$<$	2,5 V

    gate 2;

I_D = 20 μA; V_{DS} = 15 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	$<$	2,0 V

Drain-source cut-off voltage

V_{DS} = 15 V; V_{G2-S} = 4 V	I_{DSS}	2 to 20 mA

DYNAMIC CHARACTERISTCS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$|y_{fs}|$	$>$	15	mS
		typ.	17	mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	2,5	pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1,2	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1,0	pF
Noise figure at f = 200 MHz; G_S = 2 mS; $B_S = B_S$ opt	F	typ.	1,5	dB ←
		$<$	2,8	dB ←
Power gain at G_S = 2 mS; $B_S = B_S$ opt				
G_L = 0,5 mS; $B_L = B_L$ opt; f = 200 MHz	G_p	typ.	25	dB ←

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic microminiature envelope (SOT-143) with source and substrate interconnected and intended for v.h.f. applications in television tuners, using SMD* technology. The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

* Surface Mounted Devices.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	50	mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	300	mW
Junction temperature	T_j	max.	150	^oC
Transfer admittance at $f = 1$ kHz $I_D = 10$ mA; $V_{DS} = 15$ V; $+V_{G2\text{-}S} = 4$ V	$|y_{fs}|$	typ.	18	mS
Feedback capacitance at $f = 1$ MHz $I_D = 10$ mA; $V_{DS} = 15$ V; $+V_{G2\text{-}S} = 4$ V	C_{rs}	typ.	25	fF
Noise figure at $G_S = 2$ mS; $B_S = B_S$ opt $I_D = 10$ mA; $V_{DS} = 15$ V; $+V_{G2\text{-}S} = 4$ V; $f = 200$ MHz	F	typ.	1,0	dB

MECHANICAL DATA

Fig. 1 SOT-143.

Dimensions in mm
Marking code
BF994S = M93

TOP VIEW

7Z85014.7

BF994S

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (d.c. or average)	I_D	max.	50	mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Storage temperature	T_{stg}		−65 to 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm	$R_{th\ j\text{-}a}$	=	430	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents				
$\pm V_{G1\text{-}S}$ = 5 V; $V_{G2\text{-}S}$ = V_{DS} = 0	$\pm I_{G1\text{-}S}$	<	50	nA
$\pm V_{G2\text{-}S}$ = 5 V; $V_{G1\text{-}S}$ = V_{DS} = 0	$\pm I_{G2\text{-}S}$	<	50	nA
Gate-source breakdown voltages				
$\pm I_{G1\text{-}S}$ = 10 mA; $V_{G2\text{-}S}$ = V_{DS} = 0	$\pm V_{(BR)G1\text{-}SS}$		6,0 to 20	V
$\pm I_{G2\text{-}S}$ = 10 mA; $V_{G1\text{-}S}$ = V_{DS} = 0	$\pm V_{(BR)G2\text{-}SS}$		6,0 to 20	V
Drain current				
V_{DS} = 15 V; $V_{G1\text{-}S}$ = 0; $V_{G2\text{-}S}$ = 4 V	I_{DSS}		4 to 20	mA
Gate-source cut-off voltages				
I_D = 20 μA; V_{DS} = 15 V; $+V_{G2\text{-}S}$ = 4 V	$-V_{(P)G1\text{-}S}$	<	2,5	V
I_D = 20 μA; V_{DS} = 15 V; $V_{G1\text{-}S}$ = 0	$-V_{(P)G2\text{-}S}$	<	2,0	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 15 V; $+V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

Transfer admittance at f = 1 kHz	$|y_{fs}|$	>	15	mS
		typ.	18	mS
Input capacitance at gate 1: f = 1 MHz	$C_{ig1\text{-}s}$	typ.	2,5	pF
		<	3,0	pF
Input capacitance at gate 2: f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1,2	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1,0	pF
→ Noise figure at G_S = 2 mS ; B_S = B_S opt; f = 200 MHz	F	typ.	1,0	dB
→ Power gain at G_S = 2 mS ; B_S = B_S opt G_L = 0,5 mS; B_L = B_L opt; f = 200 MHz	G_p	typ.	25	dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic microminiature envelope, with source and substrate interconnected, intended for u.h.f. applications, such as television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current (average)	$I_{D(AV)}$	max.	30	mA
Total power dissipation up to $T_{amb} = 60\ ^oC$	P_{tot}	max.	200	mW
Junction temperature	T_j	max.	150	^oC
Transfer admittance at f = 1 kHz				
$I_D = 10$ mA; $V_{DS} = 15$ V; $+ V_{G2-S} = 4$ V	$|y_{fs}|$	typ.	17	mS
Feedback capacitance at f = 1 MHz				
$I_D = 10$ mA; $V_{DS} = 15$ V; $+ V_{G2-S} = 4$ V	C_{rs}	typ.	25	fF
Noise figure at optimum source admittance				
$I_D = 10$ mA; $V_{DS} = 10$ V; $+ V_{G2-S} = 4$ V; f = 800 MHz	F	typ.	2,8	dB
$I_D = 10$ mA; $V_{DS} = 15$ V; $+ V_{G2-S} = 4$ V; f = 200 MHz	F	typ.	1,5	dB

MECHANICAL DATA   Dimensions in mm   Marking code

Fig. 1 SOT-143.   BF996 = M96

TOP VIEW

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (average)	$I_{D(AV)}$	max.	30	mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10	mA
Total power dissipation up to $T_{amb} = 60\ ^oC^*$	P_{tot}	max.	200	mW
Storage temperature	T_{stg}	-65 to $+150$	^oC	
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j-a}$	=	460	K/W

Fig. 2 Power derating curve.

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

STATIC CHARACTERISTICS

T_{amb} = 25 ^oC unless otherwise specified

Gate cut-off currents

gate 1;
$\pm V_{G1\text{-}S}$ = 5 V; $V_{G2\text{-}S}$ = V_{DS} = 0 $\pm I_{G1\text{-}SS}$ <   50 nA

gate 2;
$\pm V_{G2\text{-}S}$ = 5 V; $V_{G1\text{-}S}$ = V_{DS} = 0 $\pm I_{G2\text{-}SS}$ <   50 nA

Gate-source breakdown voltages

gate 1;
$\pm I_{G1\text{-}SS}$ = 10 mA; $V_{G2\text{-}S}$ = V_{DS} = 0 $\pm V_{(BR)G1\text{-}SS}$ 6 to 20 V

gate 2;
$\pm I_{G2\text{-}SS}$ = 10 mA; $V_{G1\text{-}S}$ = V_{DS} = 0 $\pm V_{(BR)G2\text{-}SS}$ 6 to 20 V

Gate-source cut-off voltages

gate 1;
I_D = 20 μA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V $-V_{(P)G1\text{-}S}$ <   2,5 V

gate 2;
I_D = 20 μA; V_{DS} = 15 V; $V_{G1\text{-}S}$ = 0 $-V_{(P)G2\text{-}S}$ <   2,0 V

Drain-source cut-off voltage
V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V I_{DSS} 2 to 20 mA

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 ^oC

Transfer admittance at f = 1 kHz	$|y_{fs}|$	>	15 mS
		typ.	17 mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	2,2 pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1,1 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0,8 pF

Noise figure
at G_S = 2 mS; B_S = B_S opt; f = 200 MHz   F   typ.   1,5 dB

at G_S = 2 mS; B_S = B_S opt; f = 800 MHz   F   typ.   2,8 dB
                                                                                    <   3,9 dB

Power gain
G_S = 2 mS; B_S = B_S opt; G_L = 0,5 mS;
B_L = B_L opt; f = 200 MHz G_p typ.   25 dB

G_S = 2 mS; B_S = B_S opt; G_L = 1,0 mS;
B_L = B_L opt; f = 800 MHz G_p typ.   18 dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic microminiature envelope (SOT-143) with source and substrate interconnected and intended for u.h.f. applications in television tuners, using SMD* technology. The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

* Surface Mounted Devices

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	30	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; +V_{G2-S} = 4 V	$|y_{fs}|$	typ.	18	mS
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; +V_{G2-S} = 4 V	C_{rs}	typ.	25	fF
Noise figure at G_S = 3,3 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; +V_{G2-S} = 4 V; f = 800 MHz	F	typ.	1,8	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-143.

Marking code
BF996S = M95

7Z85014.7

TOP VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (d.c. or average)	I_D	max.	30	mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	300	mW
Storage temperature	T_{stg}		−65 to 150	^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to ambient in free air mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm	$R_{th\ j\text{-}a}$	=	430	K/W

STATIC CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Gate cut-off currents				
$\pm V_{G1\text{-}S} = 5$ V, $V_{G2\text{-}S} = V_{DS} = 0$	$\pm I_{G1\text{-}S}$	$<$	50	nA
$\pm V_{G2\text{-}S} = 5$ V; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm I_{G2\text{-}S}$	$<$	50	nA
Gate-source breakdown voltages				
$\pm I_{G1\text{-}S} = 10$ mA; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G1\text{-}SS}$		6,0 to 20	V
$\pm I_{G2\text{-}S} = 10$ mA; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G2\text{-}SS}$		6,0 to 20	V
Drain current				
$V_{DS} = 15$ V; $V_{G1\text{-}S} = 0$; $V_{G2\text{-}S} = 4$ V	I_{DSS}		4 to 20	mA
Gate-source cut-off voltages				
$I_D = 20\ \mu A$; $V_{DS} = 15$ V; $+V_{G2\text{-}S} = 4$ V	$-V_{(P)G1\text{-}S}$	$<$	2,5	V
$I_D = 20\ \mu A$; $V_{DS} = 15$ V; $V_{G1\text{-}S} = 0$	$-V_{(P)G2\text{-}S}$	$<$	2,0	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10$ mA; $V_{DS} = 15$ V; $+V_{G2\text{-}S} = 4$ V; $T_{amb} = 25\ ^oC$.

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	$>$ typ.	15 18	mS mS
Input capacitance at gate 1: f = 1 MHz	$C_{ig1\text{-}s}$	typ. $<$	2,3 2,6	pF pF
Input capacitance at gate 2: f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1,2	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0,8	pF
→ Noise figure f = 200 MHz; $G_S = 2$ mS; $B_S = B_S$ opt f = 800 MHz; $G_S = 3,3$ mS; $B_S = B_S$ opt	F	typ. typ.	1,0 1,8	dB dB
→ Power gain f = 200 MHz; $G_S = 2$ mS; $B_S = B_S$ opt; $G_L = 0,5$ mS; $B_L = B_L$ opt f = 800 MHz; $G_S = 3,3$ mS; $B_S = B_S$ opt; $G_L = 1,0$ mS; $B_L = B_L$ opt	G_p	typ. typ.	25 18	dB dB

DEVELOPMENT DATA

This data sheet contains advance information and
specifications are subject to change without notice.

BF997

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic microminiature envelope with source and substrate interconnected, intended for u.h.f. and v.h.f. applications, such as u.h.f./v.h.f. television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source and has an integrated drain resistance to suppress oscillation in the frequency range higher than 1 GHz.

This device is especially intended for use in pre-amplifiers in CATV tuners with a great tuning range up to 500 MHz.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current (average)	$I_{D(AV)}$	max.	30	mA
Total power dissipation up to $T_{amb} = 25\,^{\circ}C$	P_{tot}	max.	300	mW
Junction temperature	T_j	max.	150	$^{\circ}C$
Transfer admittance at $f = 1\,kHz$ $I_D = 10\,mA; V_{DS} = 15\,V; + V_{G2-S} = 4\,V$	$|y_{fs}|$	typ.	18	mS
Feedback capacitance at $f = 1\,MHz$ $I_D = 10\,mA; V_{DS} = 15\,V; + V_{G2-S} = 4\,V$	C_{rs}	typ.	25	fF
Noise figure at $G_S = 2\,mS; B_S = B_S$ opt $I_D = 10\,mA; V_{DS} = 15\,V; + V_{G2-S} = 4\,V; f = 200\,MHz$	F	typ.	1,0	dB

MECHANICAL DATA

Dimensions in mm

Marking code:
M83

Fig. 1 SOT-143.

TOP VIEW

7Z85014.7

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (average)	$I_{D(AV)}$	max.	30	mA
Gate 1 source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	300	mW
Storage temperature	T_{stg}	−65 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\,j\text{-}a}$	=	430	K/W

7Z81016.1

Fig. 2 Power derating curve.

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

STATIC CHARACTERISTICS

$T_{amb} = 25\ ^{o}C$ unless otherwise specified

Gate cut-off currents

    gate 1;

    $\pm V_{G1-S} = 5\ V; V_{G2-S} = V_{DS} = 0$ $\pm I_{G1-SS}$ $<$ 50   nA

    gate 2;

    $\pm V_{G2-S} = 5\ V; V_{G1-S} = V_{DS} = 0$ $\pm I_{G2-SS}$ $<$ 50   nA

Gate-source breakdown voltages

    gate 1;

    $\pm I_{G1-SS} = 10\ mA; V_{G2-S} = V_{DS} = 0$ $\pm V_{(BR)G1-SS}$ 6 to 20   V

    gate 2;

    $\pm I_{G2-SS} = 10\ mA; V_{G1-S} = V_{DS} = 0$ $\pm V_{(BR)G2-SS}$ 6 to 20   V

Gate-source cut-off voltages

    gate 1;

    $I_D = 20\ \mu A; V_{DS} = 15\ V; + V_{G2-S} = 4\ V$ $-V_{(P)G1-S}$ $<$ 2,5   V

    gate 2;

    $I_D = 20\ \mu A; V_{DS} = 15\ V; V_{G1-S} = 0$ $-V_{(P)G2-S}$ $<$ 2,0   V

Drain-source cut-off voltage

    $V_{DS} = 15\ V; V_{G2-S} = 4\ V; V_{G1-S} = 0$ I_{DSS} 2 to 20   mA

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10\ mA; V_{DS} = 15\ V; + V_{G2-S} = 4\ V; T_{amb} = 25\ ^{o}C$

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	$>$	15 mS
		typ.	18 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	2,5 pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1,2 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1,0 pF
Noise figure at f = 200 MHz; G_S = 2 mS; B_S = B_S opt	F	typ.	1,0 dB ◄—
Power gain at G_S = 2 mS; B_S = B_S opt ◄—			
G_L = 0,5 mS; = B_L = B_L opt; f = 200 MHz	G_p	typ.	25 dB ◄—

DEVELOPMENT DATA

SILICON N-CHANNEL DUAL IG-MOS-FET

Depletion type field-effect transistor in a TO-72 metal envelope with source and substrate connected to the case, intended for a wide range of v.h.f. applications, such as v.h.f. television tuners, f.m. tuners, as well as for applications in communication, instrumentation and control.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

The tetrode configuration, a series arrangement of two gate controlled channels, offers:
a) very low feedback capacitance providing the possibility of more than 40 dB gain control in r.f. amplifiers requiring negligible a.g.c. power.
b) excellent signal handling capability over the entire gain control range.
c) low noise figure combined with high gain.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	50	mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	300	mW
Junction temperature	T_j	max.	175	^oC
Transfer admittance at f = 1 kHz $I_D = 10\ mA; V_{DS} = 10\ V; + V_{G2-S} = 4\ V$	$\|y_{fs}\|$	typ.	15	mS
Feedback capacitance at f = 1 MHz $I_D = 10\ mA; V_{DS} = 10\ V; + V_{G2-S} = 4\ V$	C_{rs}	typ.	30	fF
Noise figure at optimum source admittance $I_D = 10\ mA; V_{DS} = 10\ V; + V_{G2-S} = 4\ V$ $G_S = 1,2\ mS; -B_S = 5,7\ mS; f = 200\ MHz$	F	typ.	2,3	dB

MECHANICAL DATA   Dimensions in mm

Fig. 1 TO-72.

Source and substrate connected to the case.

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (d.c. or average)	I_D	max.	50	mA
Drain current (peak value)	I_{DM}	max.	100	mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10	mA
Total power dissipation up to T_{amb} = 25 ^{o}C	P_{tot}	max.	300	mW
Storage temperature	T_{stg}	-65 to $+175$		^{o}C
Junction temperature	T_j	max.	175	^{o}C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	500	K/W

STATIC CHARACTERISTICS T_{amb} = 25 °C unless otherwise specified

Gate cut-off currents

$\pm V_{G1-S}$ = 5 V; V_{G2-S} = V_{DS} = 0	$\pm I_{G1-SS}$	<	10	nA
$\pm V_{G1-S}$ = 5 V; V_{G2-S} = V_{DS} = 0; T_j = 150 °C	$\pm I_{G1-SS}$	<	10	μA
$\pm V_{G2-S}$ = 5 V; V_{G1-S} = V_{DS} = 0	$\pm I_{G2-SS}$	<	10	nA
$\pm V_{G2-S}$ = 5 V; V_{G1-S} = V_{DS} = 0; T_j = 150 °C	$\pm I_{G2-SS}$	<	10	μA

Gate-source breakdown voltages

$\pm I_{G1-SS}$ = 0,1 mA; V_{G2-S} = V_{DS} = 0	$\pm V_{(BR)G1-SS}$	6,0 to 20	V
$\pm I_{G2-SS}$ = 0,1 mA; V_{G1-S} = V_{DS} = 0	$\pm V_{(BR)G2-SS}$	6,0 to 20	V

Drain current

V_{DS} = 10 V; V_{G1-S} = 0; $+V_{G2-S}$ = 4 V	I_{DSS}	20 to 55	mA [1]

Gate 1-source voltage

I_D = 10 mA; V_{DS} = 10 V; $+V_{G2-S}$ = 4 V	$-V_{G1-S}$	0,6 to 2,1	V

Gate-source cut-off voltages

I_D = 10 μA ; V_{DS} = 10 V; $+V_{G2-S}$ = 4 V	$-V_{(P)G1-S}$	1,5 to 3,8	V
I_D = 10 μA ; V_{DS} = 10 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	1,5 to 3,4	V

---

[1]) Measured under pulse conditions.

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10$ mA; $V_{DS} = 10$ V; $+V_{G2-S} = 4$ V; $T_{amb} = 25$ °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	>	12	mS
		typ.	15	mS
Input capacitance at f = 1 MHz	C_{is}	typ.	5,5	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	30	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	3,5	pF

Noise figure at optimum source admittance

$G_S = 0,95$ mS; $-B_S = 5,0$ mS; f = 100 MHz	F	typ.	1,9	dB
$G_S = 1,20$ mS; $-B_S = 5,7$ mS; f = 200 MHz	F	typ.	2,3	dB
		<	3,0	dB

Cross modulation at f = 200 MHz

Wanted signal at f_o = 197,5 MHz
Unwanted signal at f_{int} = 202,5 MHz

Interference voltage at g_1 for K = 1%	V_{int}	typ.	100	mV [1]

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[1] Cross modulation is defined here as the voltage at g_1 of an unwanted signal with 80% modulation depth, giving 0,8% modulation depth on the wanted signal (a.m. definition).

$|y_{fs}|$ (mA/V)

typ

$V_{DS} = 10$ V
V_{G1-S} adjusted
for $I_D = 10$ mA
at $+V_{G2-S} = 4$ V
f = 1 kHz
$T_{amb} = 25\ ^{\circ}C$

V_{G2-S} (V)

7Z67767.1

G_S (mA/V)

F = 2,3 dB
2,5 dB
3,0 dB
3,5 dB
4,0 dB
4,5 dB
5,0 dB

B_S (mA/V)

typ. values
f = 200 MHz
$I_D = 10$ mA
$V_{DS} = 10$ V
$+V_{G2-S} = 4$ V
$T_{amb} = 25\ ^{\circ}C$

7Z67773.1
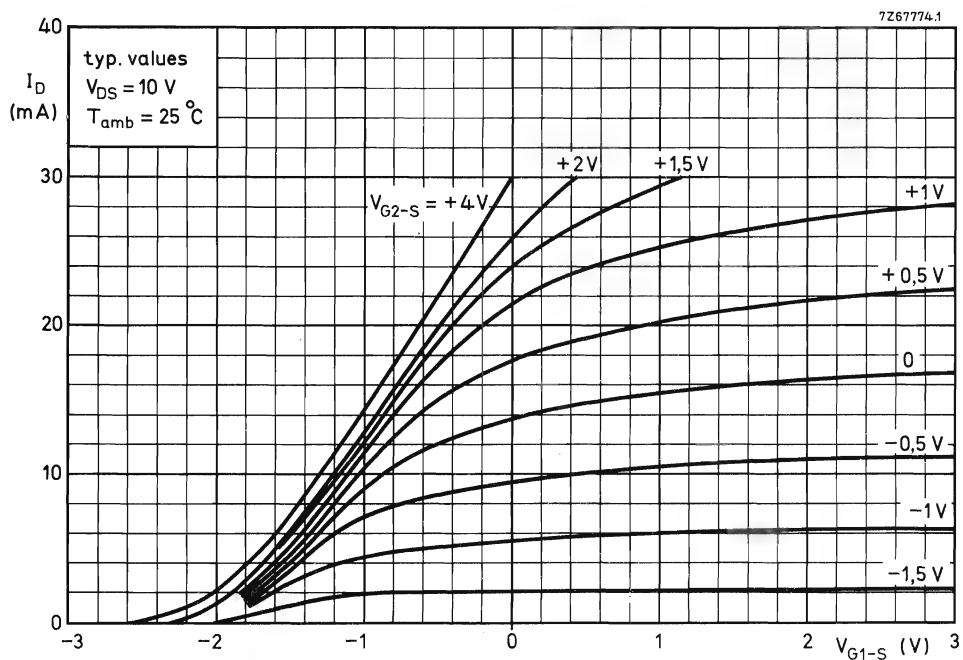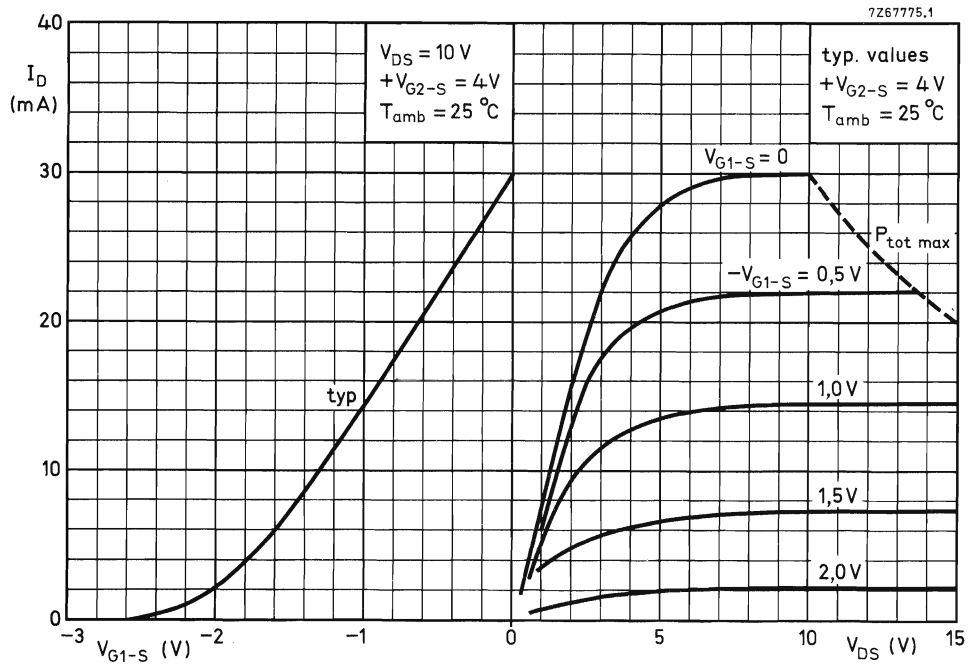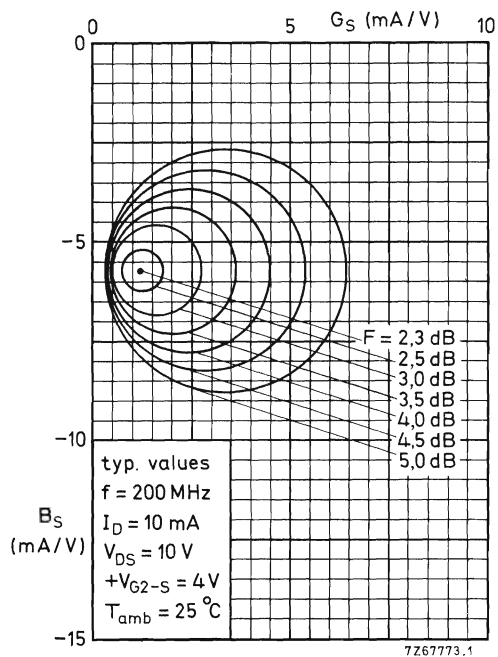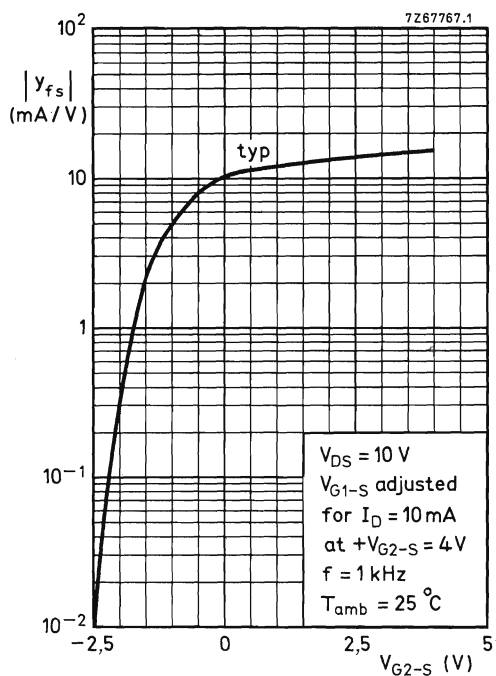
circles of constant noise figure

DEVICE DATA

VERTICAL DMOS-FETS

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use as line current interuptor in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage	V_{GS}	max.	15	V
Drain current (d.c.)	I_D	max.	120	mA
Total power dissipation up to $T_c = 25\ ^oC$	P_{tot}	max.	500	mW
Junction temperature	T_j	max.	150	^oC
Drain-source ON-resistance $V_{GS} = 2{,}6$ V; $I_D = 20$ mA	R_{DSon}	max.	28	Ω
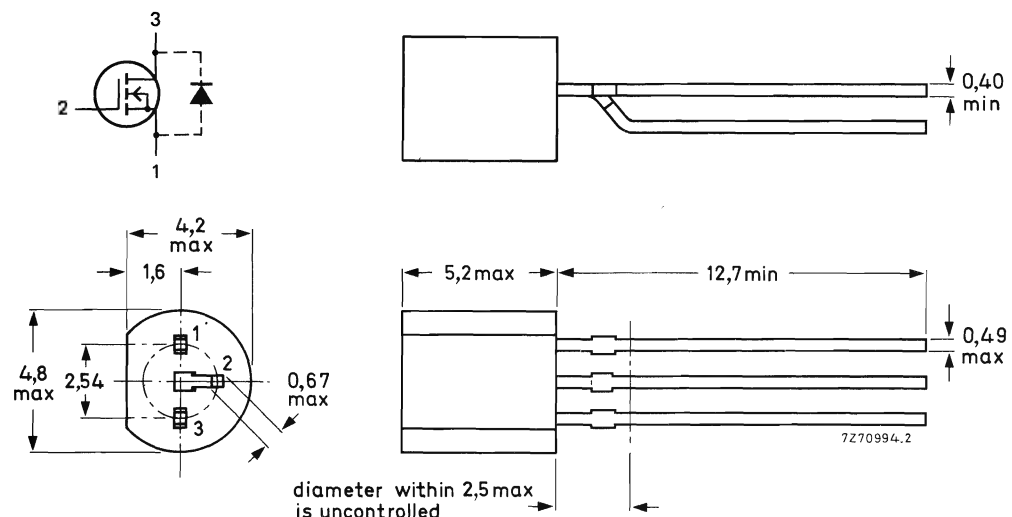
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

diameter within 2,5 max is uncontrolled

Note: Various pinnings are available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DSS}	max.	200	V
Drain-gate voltage	V_{DGS}	max.	200	V
Gate-source voltage	V_{GS}	max.	15	V
Drain current (d.c.)	I_D	max.	120	mA
Total power dissipation up to $T_c = 25\ ^oC$	P_{tot}	max.	500	mW
Storage temperature	T_{stg}		−55 to +150	^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	150	K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0$; $I_D = 100\ \mu A$	$V_{(BR)DS}$	>	200	V
Gate-source leakage current $V_{GS} = 15$ V; $V_{DS} = 0$	I_{GSoff}	<	10	nA
Drain cut-off current $V_{DS} = 130$ V; $V_{GS} = 0$	I_{DSS}	<	30	nA
$V_{DS} = 70$ V; $V_{GS} = 0,2$ V	I_{DSX}	<	1	μA
Drain-source ON-resistance $V_{GS} = 2,6$ V; $I_D = 20$ mA	RDSon	typ. <	15 28	Ω Ω
$V_{GS} = 10$ V; $I_D = 250$ mA	RDSon	typ.	6	Ω
Gate threshold voltage $I_D = 1$ mA; $V_{DS} = V_{GS}$	$V_{GS(th)}$	> typ. <	0,8 1,8 2,8	V V V
Transfer admittance at f = 1 kHz $I_D = 250$ mA; $V_{DS} = 15$ V	$|y_{fs}|$	typ.	250	mS
Input capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{is}	typ.	70	pF
Output capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{os}	typ.	20	pF
Feedback capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{rs}	typ.	5	pF
Switching times (see Figs 2 and 3) $I_D = 250$ mA; $V_{DS} = 50$ V; $V_{GS} = 0$ to 10 V	t_{on}	typ. <	4 10	ns ns
	t_{off}	typ. <	15 25	ns ns

Fig. 2 Switching times test circuit.

Fig. 3 Input and output waveforms.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features:

- Very low R_{DSon}.
- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	60	V
Gate-source voltage	V_{GS}	max.	15	V
Drain current (d.c.)	I_D	max.	500	mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	830	mW
Junction temperature	T_j	max.	150	^oC
Drain-source ON-resistance $V_{GS} = 10$ V; $I_D = 200$ mA	R_{DSon}	max.	5	Ω
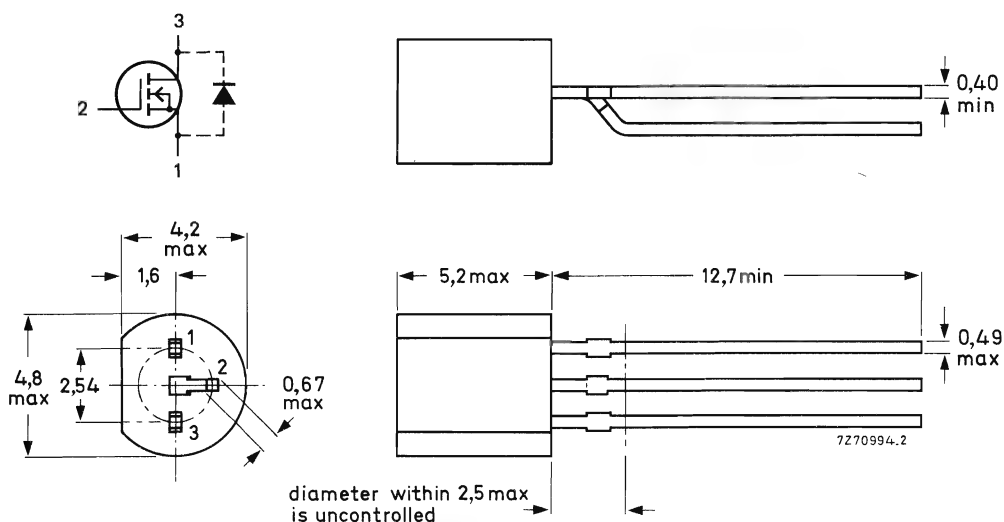
MECHANICAL DATA   Dimensions in mm

Fig. 1 TO-92 variant.

diameter within 2,5 max is uncontrolled

Note: Various pinnings are available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	60	V
Drain-gate voltage	V_{DG}	max.	60	V
Gate-source voltage	V_{GS}	max.	15	V
Drain current (d.c.) at T_c = 25 $^{\circ}$C	I_D	max.	500	mA
Total power dissipation up to T_{amb} = 25 $^{\circ}$C	P_{tot}	max.	830	mW
Storage temperature	T_{stg}		-55 to $+150$	$^{\circ}$C
Junction temperature	T_j	max.	150	$^{\circ}$C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	150	K/W

CHARACTERISTICS

T_j = 25 $^{\circ}$C unless otherwise specified

|				
Drain-source breakdown voltage V_{GS} = 0; I_D = 100 μA	$V_{(BR)DS}$	$>$ typ.	60 90	V V
Gate threshold voltage V_{GS} = V_{DS}; I_D = 1 mA	$V_{GS(th)}$	$>$ $<$	0,8 3,0	V V
Gate-source leakage current V_{GS} = 15 V; V_{DS} = 0	I_{GSoff}	$<$	10	nA
Drain cut-off current V_{DS} = 25 V; V_{GS} = 0	I_{DSS}	$<$	0,5	μA
Drain-source ON-resistance * V_{GS} = 10 V; I_D = 200 mA	R_{DSon}	typ. $<$	2,5 5,0	Ω Ω
Forward transconductance * V_{DS} = 10 V; I_D = 200 mA; f = 1 kHz	g_{fs}	typ.	200	mS
Capacitances at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. $<$	25 40	pF pF
	C_{os}	typ. $<$	22 30	pF pF
	C_{rs}	typ. $<$	6 10	pF pF
Switching times at I_D = 200 mA I_D = 200 mA; V_{DS} = 50 V;	t_{on}	typ. $<$	4 10	ns ns
V_{GS} = 0 to 10 V	t_{off}	typ. $<$	4 10	ns ns

* t_p = 80 μs; δ = 0,01.

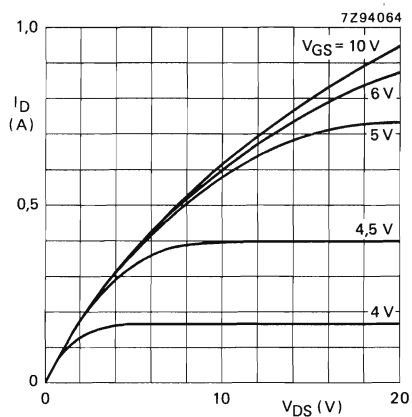Fig. 2 Switching times test circuit

Fig. 3 Input and output waveforms

P-CHANNEL VERTICAL D-MOS TRANSISTOR

P-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Very low R_{DSon}
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	45	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	20	V
Drain current (d.c.)	$-I_D$	max.	0,25	A
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	0,83	W
Drain-source ON-resistance $-I_D = 200$ mA; $-V_{GS} = 10$ V	R_{DSon}	typ. <	9 14	Ω Ω
Transfer admittance at f = 1 kHz $-I_D = 200$ mA; $-V_{DS} = 15$ V	$\|y_{fs}\|$	typ.	125	mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

diameter within 2,5 max is uncontrolled

7Z70994.2

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	45 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	20 V
Drain current (d.c.)	$-I_D$	max.	0,25 A
Drain current (peak value)	$-I_{DM}$	max.	0,5 A
Total power dissipation up to $T_{amb} = 25\,^oC*$	P_{tot}	max.	0,83 W
Storage temperature	T_{stg}		-65 to $+150$ ^oC
Junction temperature	T_j	max.	150 ^oC

THERMAL RESISTANCE

From junction to ambient*	$R_{th\,j\text{-}a}$	=	150 K/W

CHARACTERISTICS

$T_j = 25\,^oC$ unless otherwise specified

Drain-source breakdown voltage $-I_D = 100\,\mu A$; $V_{GS} = 0$	$-V_{(BR)DS}$	min.	45 V
Drain-source leakage current $-V_{DS} = 25$ V; $V_{GS} = 0$	$-I_{DSS}$	max.	0,5 μA
Gate-source leakage current $-V_{GS} = 15$ V; $V_{DS} = 0$	$-I_{GSS}$	max.	20 nA
Gate threshold voltage $-I_D = 1$ mA; $V_{DS} = V_{GS}$	$-V_{GS(th)}$	min. max.	1,0 V 3,5 V
Drain-source ON-resistance $-I_D = 200$ mA; $-V_{GS} = 10$ V	R_{DSon}	typ. max.	9 Ω 14 Ω
Transfer admittance at f = 1 kHz $-I_D = 200$ mA; $-V_{DS} = 15$ V	$|y_{fs}|$	typ.	125 mS
Input capacitance at f = 1 MHz $-V_{DS} = 10$ V; $V_{GS} = 0$	C_{is}	typ. <	30 pF 45 pF
Output capacitance at f = 1 MHz $-V_{DS} = 10$ V; $V_{GS} = 0$	C_{os}	typ. <	20 pF 30 pF
Feedback capacitance at f = 1 MHz $-V_{DS} = 10$ V; $V_{GS} = 0$	C_{rs}	typ. <	5 pF 10 pF
Switching times (see Figs 2 and 3) $-I_D = 200$ mA; $-V_D = 40$ V; $-V_{GS} = 0$ to 10 V	t_{on} t_{off}	typ. typ.	4 ns 10 ns

* Transistor mounted on printed-circuit board, max. lead length 4 mm.

Fig. 2 Switching times test circuit.

Fig. 3 Input and output waveforms.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features:

- Very low R_{DSon}
- Direct interface to C-MOS, TTL, etc.
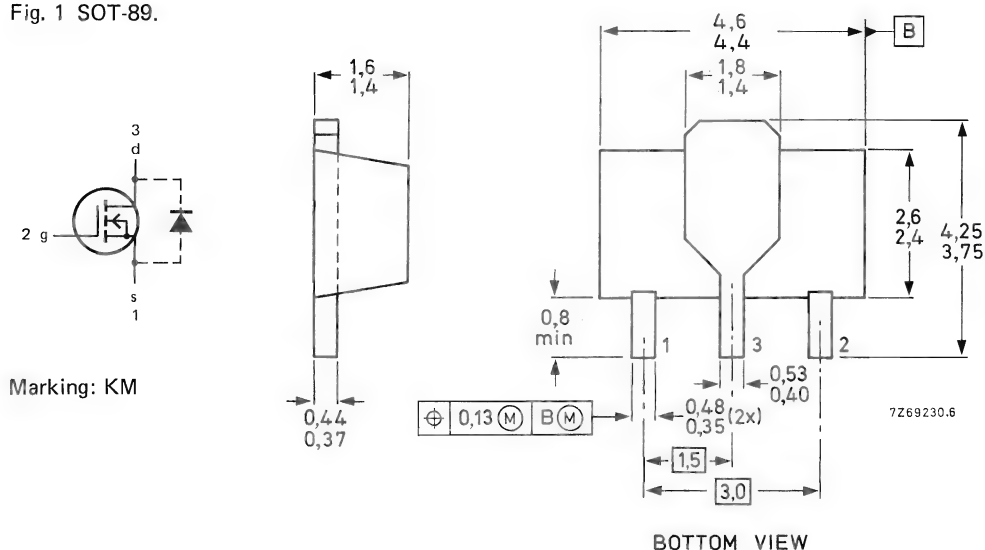- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	0,5	A
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	1	W
Drain-source ON-resistance $I_D = 500$ mA; $V_{GS} = 10$ V	R_{DSon}	typ. max.	2 4	Ω Ω
Transfer admittance $I_D = 500$ mA; $V_{DS} = 15$ V; $f = 1$ kHz	$|Y_{fs}|$	typ.	300	mS

MECHANICAL DATA   Dimensions in mm

Fig. 1 TO-92 variant.

diameter within 2,5max
is uncontrolled

Note: Various pinnings are available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	0,5	A
Drain current (peak)	I_{DM}	max.	1,0	A
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	1	W
Storage temperature	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\,j\text{-}a}$	125	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DS}$	>	80	V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	<	10	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	<	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	> <	1,5 3,5	V V
Drain-source ON-resistance (see Fig. 4) I_D = 500 mA; V_{GS} = 10 V	R_{DSon}	typ. <	2,0 4,0	Ω Ω
Transfer admittance at f = 1 kHz I_D = 500 mA; V_{DS} = 15 V	$|y_{fs}|$	typ.	300	mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{is}	typ. <	45 60	pF pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{os}	typ. <	30 45	pF pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ. <	8 12	pF pF
Switching times (see Figs 2 and 3) I_D = 500 mA; V_{DS} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	< <	10 15	ns ns

* Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

Fig. 2 Switching times test circuit.

Fig. 3 Input and output waveforms.

Fig. 4 T_j = 25 °C; typical values.

Fig. 5 T_j = 25 °C; typical values at V_{DS} = 10 V.

Fig. 6 T_j = 25 °C; typical values.
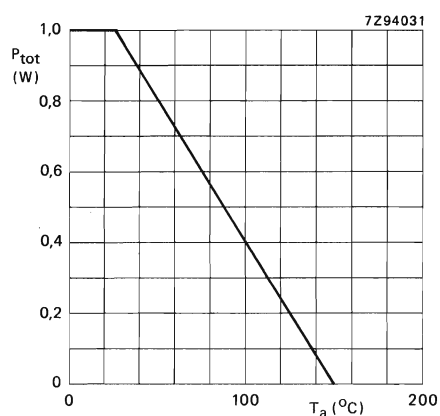
Fig. 7 Power derating curve.
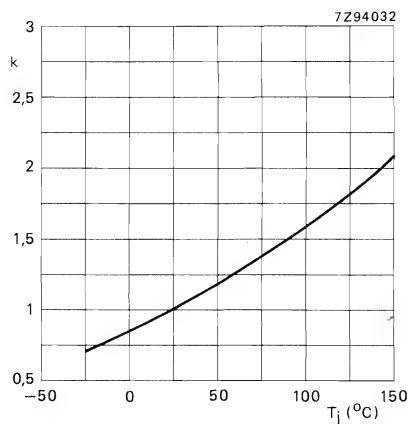
Fig. 8 $k = \dfrac{R_{DS\ on}\ \text{at}\ T_j}{R_{DS\ on}\ \text{at}\ 25\ ^oC}$; typ. values at 500 mA/10 V.
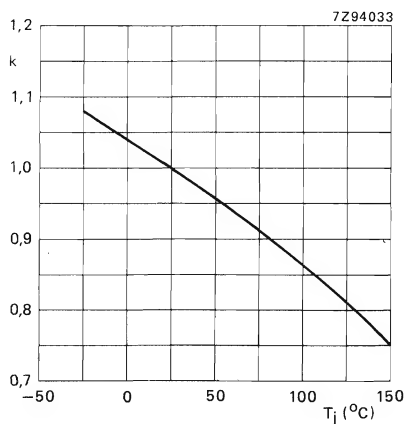
Fig. 9 $k = \dfrac{V_{GS(th)}\ \text{at}\ T_j}{V_{GS(th)}\ \text{at}\ 25\ ^oC}$; $V_{GS(th)}$ at 1 mA; typical values.
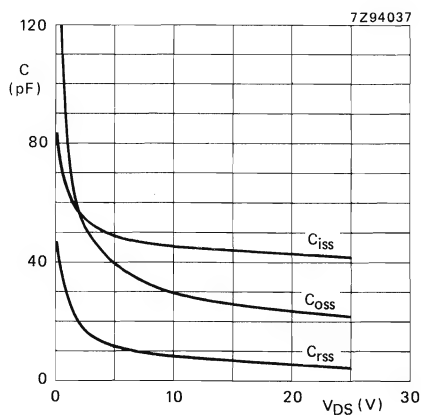
Fig. 10 T_j = 25 ^oC; V_{GS} = 0; f = 1 MHz; typical values.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use in telephone ringer circuits and for application with relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	300	mA
Total power dissipation up to $T_{amb} = 25\ ^{\circ}C$	P_{tot}	max.	0,83	W
Drain-source ON-resistance $I_D = 150$ mA; $V_{GS} = 5$ V	R_{DSon}	typ. max.	7 10	Ω Ω
Transfer admittance $I_D = 200$ mA; $V_{DS} = 5$ V; $f = 1$ kHz	$|y_{fs}|$	typ.	150	mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

diameter within 2,5 max is uncontrolled

Note: Various pinnings are available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	300	mA
Drain current (peak)	I_{DM}	max.	600	mA
Total power dissipation up to $T_{amb} = 25$ °C*	P_{tot}	max.	0,83	W
Storage temperature	T_{stg}		-65 to $+150$	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\,j\text{-}a}$		150	K/W

CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified

Drain-source breakdown voltage $I_D = 100\ \mu A$; $V_{GS} = 0$	$V_{(BR)DS}$	$>$	80	V
Drain-source leakage current $V_{DS} = 60$ V; $V_{GS} = 0$	I_{DSS}	$<$	1,0	μA
Gate-source leakage current $V_{GS} = 20$ V; $V_{DS} = 0$	I_{GSS}	$<$	100	nA
Gate threshold voltage $I_D = 1$ mA; $V_{DS} = V_{GS}$	$V_{GS(th)}$	$>$ $<$	1,5 3,5	V V
Drain-source ON-resistance (see Fig. 4) $I_D = 150$ mA; $V_{GS} = 5$ V	R_{DSon}	typ. $<$	7 10	Ω Ω
Transfer admittance at f = 1 kHz $I_D = 200$ mA; $V_{DS} = 5$ V	$|y_{fs}|$	typ.	150	mS
Input capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{is}	typ. $<$	15 30	pF pF
Output capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{os}	typ. $<$	13 20	pF pF
Feedback capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{rs}	typ. $<$	3 6	pF pF
Switching times (see Figs 2 and 3) $I_D = 200$ mA; $V_{DS} = 50$ V; $V_{GS} = 0$ to 10 V	t_{on}	typ. $<$	4 10	ns ns
	t_{off}	typ. $<$	4 10	ns ns

* Transistor mounted on printed circuit board, max. lead length 4 mm.
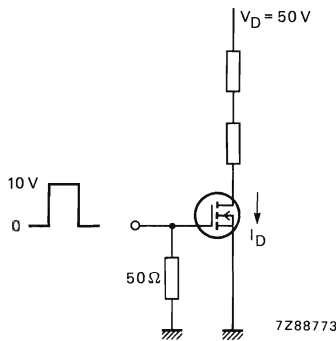
Fig. 2 Switching times test circuit.
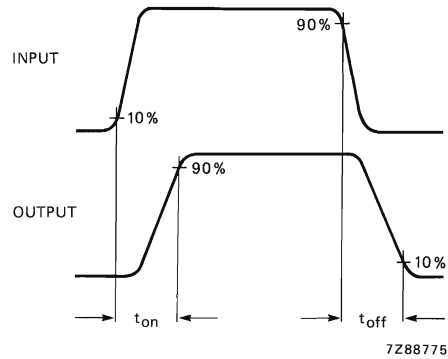
Fig. 3 Input and output waveforms.
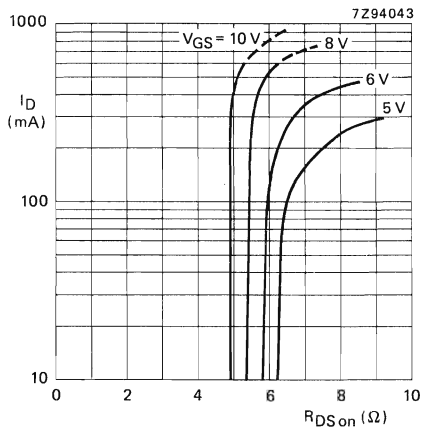
Fig. 4 T_j = 25 °C; typical values.
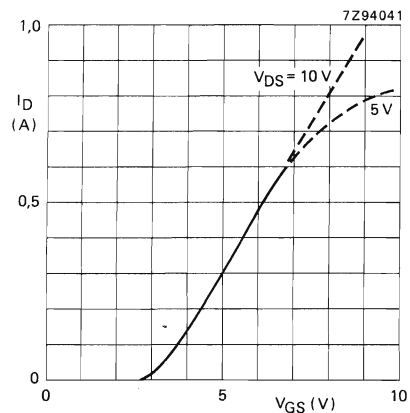
Fig. 5 T_j = 25 °C; typical values.
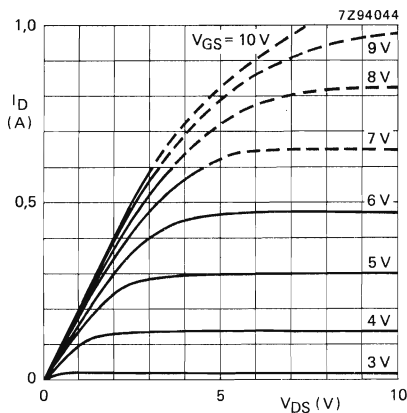
Fig. 6 T_j = 25 °C; typical values.
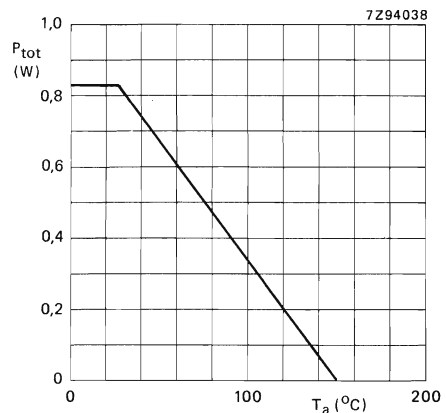
Fig. 7 Power derating curve.
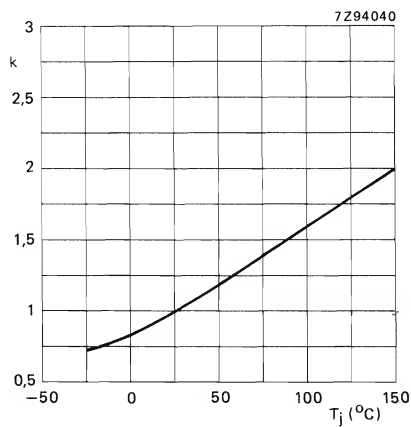
Fig. 8 $k = \dfrac{R_{DS\ on}\ at\ T_j}{R_{DS\ on}\ at\ 25\ ^oC}$; typ. values
at 150 mA/5 V.

Fig. 9 $k = \dfrac{V_{GS(th)}\ at\ T_j}{V_{GS(th)}\ at\ 25\ ^oC}$; $V_{GS(th)}$ at 1 mA;
typical values.

Fig. 10 T_j = 25 ^oC; V_{GS} = 0; f = 1 MHz; typical values.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	250 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	6 Ω 12 Ω
Transfer admittance I_D = 250 mA; V_{DS} = 15 V; f = 1 kHz	$|y_{fs}|$	typ.	250 mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

diameter within 2,5 max is uncontrolled

7Z70994.2

Note: Various pinnings are available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	250	mA
Drain current (peak)	I_{DM}	max.	800	mA
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	1	W
Storage temperature	T_{stg}	−65 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\,j\text{-}a}$	125	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DS}$	$>$	200	V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	$<$	10	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	$<$	100	nA
Gate threshold voltage I_D = 1 mA; $V_{DS} = V_{GS}$	$V_{GS(th)}$	$>$ $<$	0,8 2,8	V V
Drain-source ON-resistance (see Fig. 4) I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. $<$	6 12	Ω Ω
Transfer admittance at f = 1 kHz I_D = 250 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250	mS
Input capacitance at f = 1 MHz $\rightarrow$ V_{DS} = 10 V; V_{GS} = 0	C_{is}	typ. $<$	70 90	pF pF
Output capacitance at f = 1 MHz $\rightarrow$ V_{DS} = 10 V; V_{GS} = 0	C_{os}	typ. $<$	20 30	pF pF
Feedback capacitance at f = 1 MHz $\rightarrow$ V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ. $<$	5 10	pF pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DS} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ. $<$	4 10	ns ns
	t_{off}	typ. $<$	15 25	ns ns

* Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for collector lead min. 10 mm x 10 mm.
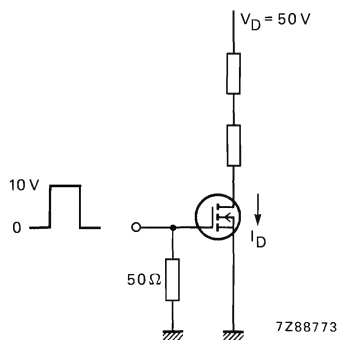
Fig. 2 Switching times test circuit.
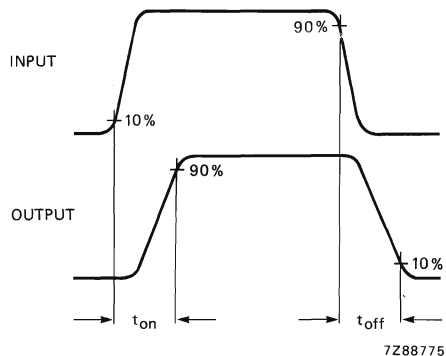
Fig. 3 Input and output waveforms.
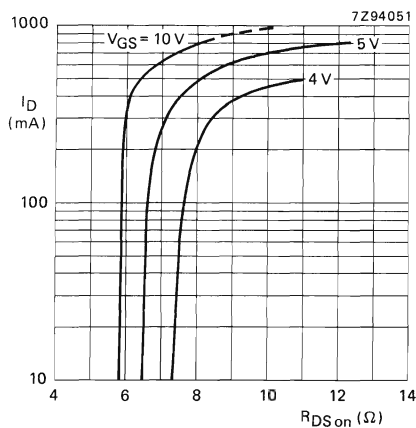
Fig. 4 T_j = 25 °C; typical values.
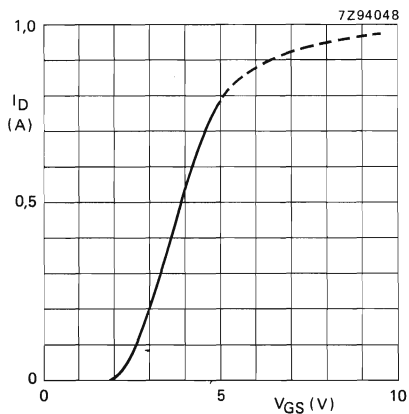
Fig. 5 T_j = 25 °C; V_{DS} = 10 V; typical values.
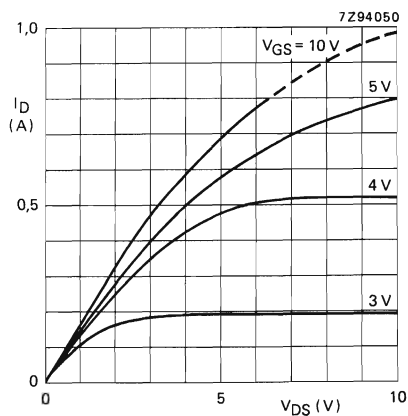
Fig. 6 T_j = 25 °C; typical values.
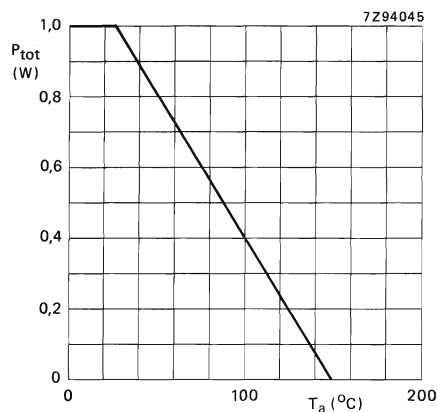
Fig. 7 Power derating curve.
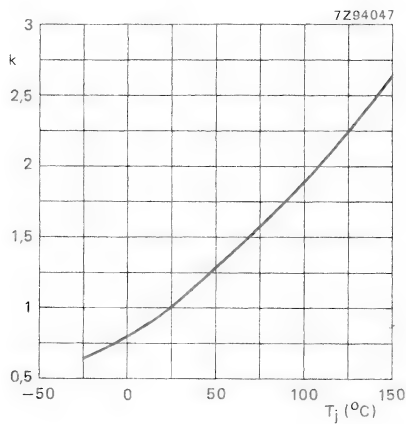
Fig. 8 $k = \dfrac{R_{DS \, on} \text{ at } T_j}{R_{DS \, on} \text{ at } 25 \, ^oC}$; at 400 mA/10 V; typical values.

Fig. 9 $k = \dfrac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25 \, ^oC}$; $V_{GS(th)}$ at 1 mA; typical values.

Fig. 10 $T_j = 25 \, ^oC$; $V_{GS} = 0$; f = 1 MHz; typical values.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	180	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	200	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	300	mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	1	W
Drain-source ON-resistance $\qquad I_D = 15$ mA; $V_{GS} = 3$ V	R_{DSon}	typ. max.	7 10	Ω Ω
Transfer admittance $\qquad I_D = 300$ mA; $V_{DS} = 15$ V; f = 1 kHz	$|y_{fs}|$	typ.	250	mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:
1 = source
2 = gate
3 = drain

diameter within 2,5 max is uncontrolled

Note: Various pinnings are available on request.

BST76A

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	180	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant$ 2 ms)	$V_{DS(SM)}$	max.	200	V
Gate source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	300	mA
Drain current (peak)	I_{DM}	max.	800	mA
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	1	W
Storage temperature	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient*	$R_{th j-a}$	125	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DS}$	>	180	V
Drain-source leakage current V_{DS} = 120 V; V_{GS} = 0	I_{DSS}	<	10	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	<	100	nA
Gate threshold voltage I_D = 100 μA; V_{DS} = V_{GS}	$V_{GS(th)}$	> <	0,7 2,4	V V
Drain-source ON-resistance (see Fig. 4) I_D = 15 mA; V_{GS} = 3 V	R_{DSon}	typ. <	7 10	Ω Ω
I_D = 300 mA; V_{GS} = 10 V	R_{DSon}	typ.	6	Ω
Transfer admittance at f = 1 kHz I_D = 300 mA; V_{DS} = 15 V	$|y_{fs}|$	typ.	250	mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{is}	typ. <	50 65	pF pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{os}	typ. <	20 30	pF pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ. <	6 10	pF pF
Switching times (see Figs 2 and 3) I_D = 300 mA; V_{DS} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	< <	10 15	ns ns

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* Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.
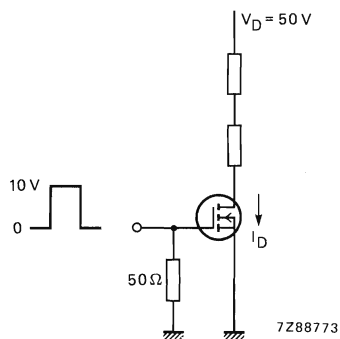
Fig. 2 Switching times test circuit.
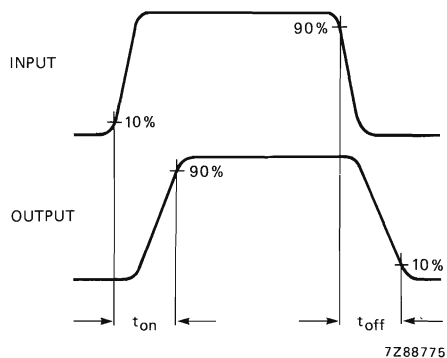
Fig. 3 Input and output waveforms.
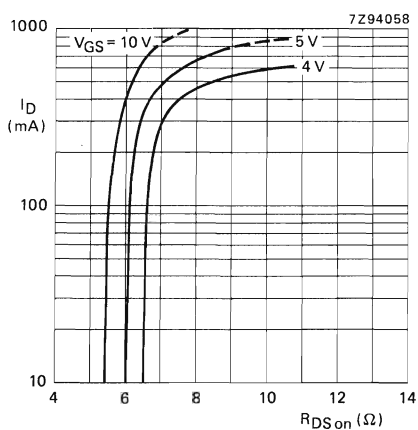
Fig. 4 T_j = 25 °C; typical values.
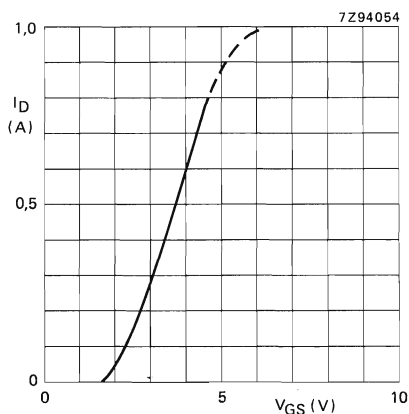
Fig. 5 T_j = 25 °C; V_{DS} = 10 V; typ. values.
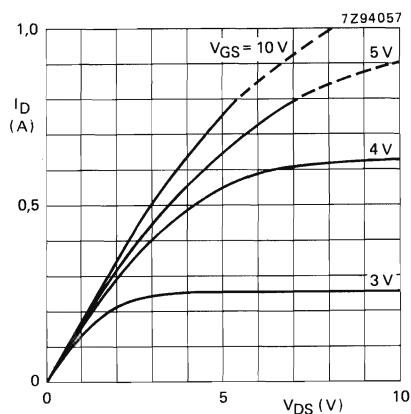
Fig. 6 T_j = 25 °C; typical values.
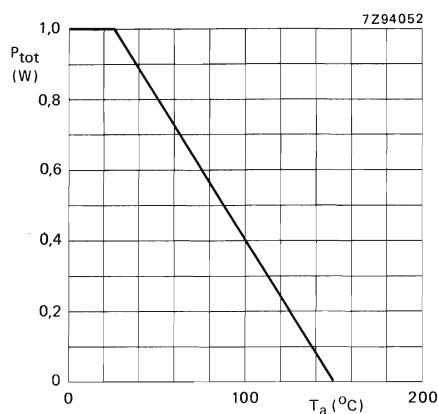
Fig. 7 Power derating curve.
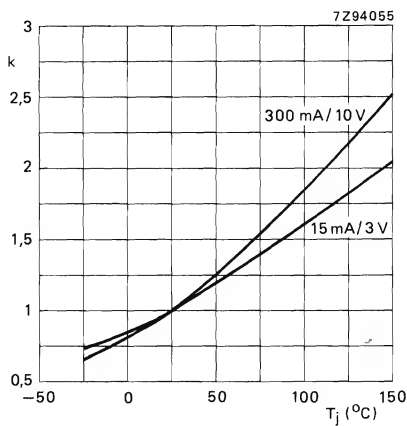
Fig. 8 $k = \dfrac{R_{DS\ on}\ at\ T_j}{R_{DS\ on}\ at\ 25\ ^oC}$; typical values.
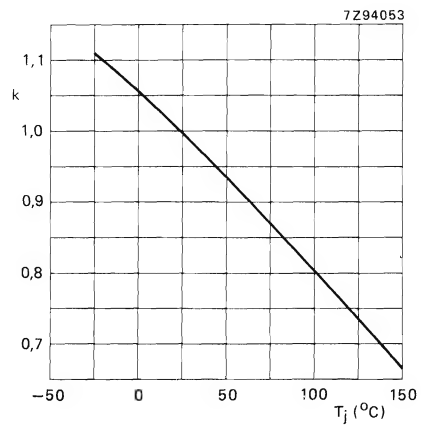
Fig. 9 $k = \dfrac{V_{GS(th)}\ at\ T_j}{V_{GS(th)}\ at\ 25\ ^oC}$; $V_{GS(th)}$ at 0,1 mA; typical values.
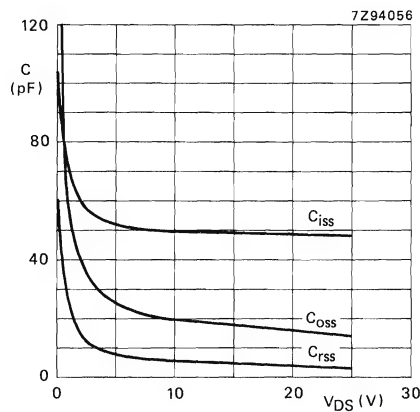
Fig. 10 T_j = 25 ^oC; V_{GS} = 0; f = 1 MHz; typical values.

HIGH-VOLTAGE N-CHANNEL VERTICAL D-MOS TRANSISTOR

High-voltage N-channel vertical D-MOS transistor in plastic TO-126 envelope and intended for use in relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching, low power switching losses
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	450 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 50\ \mu s$)	$V_{DS(SM)}$	max.	525 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	0,75 A
Total power dissipation up to $T_{mb} = 75\ ^oC$	P_{tot}	max.	15 W
Drain-source ON-resistance $\quad I_D = 500$ mA; $V_{GS} = 10$ V	R_{DSon}	typ.	15 Ω
Transfer admittance $\quad I_D = 250$ mA; $V_{DS} = 20$ V; f = 1 kHz	$\lvert y_{fs} \rvert$	typ.	400 mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-126.

Drain connected to mounting base.

Pinning;
1 = source
2 = drain
3 = gate

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	450	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 50~\mu s$)	$V_{DS(SM)}$	max.	525	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	0,75	A
Drain current (peak)	I_{DM}	max.	1,5	A
Total power dissipation up to $T_{mb} = 75~^oC$	P_{tot}	max.	15	W
Storage temperature	T_{stg}	−65 to +150		^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to ambient	$R_{th~j-a}$	100	K/W
From junction to mounting base	$R_{th~j-mb}$	5	K/W

CHARACTERISTICS

$T_j = 25~^oC$ unless otherwise specified

Drain-source breakdown voltage $I_D = 100~\mu A$; $V_{GS} = 0$	$V_{(BR)DS}$	>	450	V
Drain-source leakage current $V_{DS} = 350$ V; $V_{GS} = 0$	I_{DSS}	<	25	μA
Gate-source leakage current $V_{GS} = 20$ V; $V_{DS} = 0$	I_{GSS}	<	100	nA
Gate-source cut-off voltage $I_D = 1$ mA; $V_{DS} = V_{GS}$	$V_{(P)GS}$	> <	2,0 4,0	V V
Drain-source ON-resistance (see Fig. 4) $I_D = 100$ mA; $V_{GS} = 10$ V	R_{DSon}	typ. <	10 14	Ω Ω
$I_D = 500$ mA; $V_{GS} = 10$ V	R_{DSon}	typ.	15	Ω
Transfer admittance at f = 1 kHz $I_D = 250$ mA; $V_{DS} = 20$ V	$|y_{fs}|$	typ.	400	mS
Input capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{is}	typ. <	75 100	pF pF
Output capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{os}	typ. <	25 35	pF pF
Feedback capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{rs}	typ. <	3 5	pF pF
Switching times (see Figs 2 and 3) $I_D = 100$ mA; $V_{DS} = 200$ V; $V_{GS} = 0$ to 10 V	t_{on}	<	10	ns
	t_{off}	<	100	ns
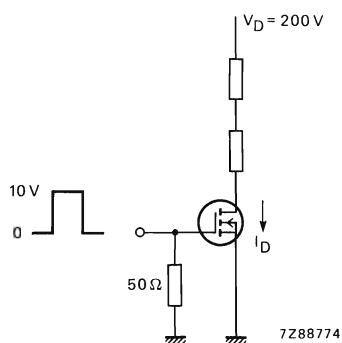
Fig. 2 Switching times test circuit.
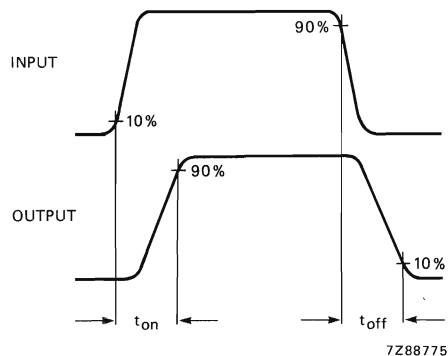
Fig. 3 Input and output waveforms.
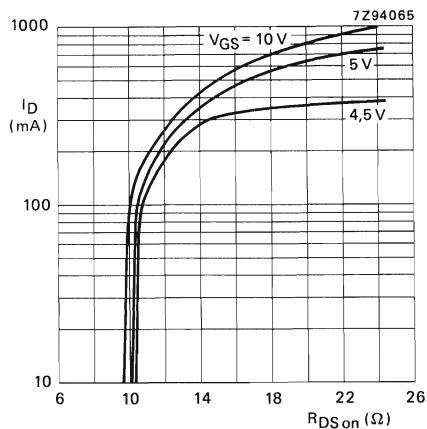
Fig. 4 T_j = 25 °C; typical values.
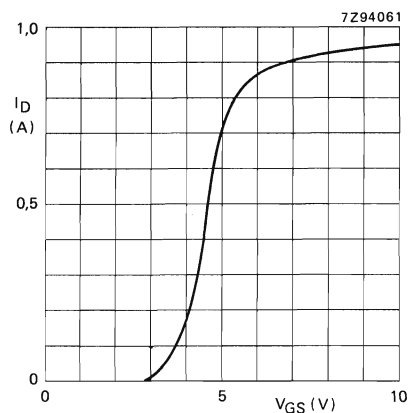
Fig. 5 T_j = 25 °C; V_{DS} = 20 V; typical values.

Fig. 6 T_j = 25 °C; typical values.

Fig. 7 Power derating curve.

Fig. 8 $k = \dfrac{R_{DS\,on}\text{ at }T_j}{R_{DS\,on}\text{ at }25\,^oC}$; typical values.

Fig. 9 $k = \dfrac{V_{GS(th)}\text{ at }T_j}{V_{GS(th)}\text{ at }25\,^oC}$; $V_{GS(th)}$ at 1 mA; typical values.

Fig. 10 $T_j = 25\,^oC$; $V_{GS} = 0$; $f = 1$ MHz; typical values.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in SOT-89 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for application with relay, high-speed and line-transformer drivers.

Features

- Very low R_{DSon}
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	0,5	A
Total power dissipation up to $T_{amb} = 25\ ^{o}C$	P_{tot}	max.	1	W
Drain-source ON-resistance $I_D = 500$ mA; $V_{GS} = 10$ V	R_{DSon}	typ. $<$	2,0 4,0	Ω Ω
Transfer admittance $I_D = 500$ mA; $V_{DS} = 15$ V; f = 1 kHz	$|y_{fs}|$	typ.	300	mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-89.

Marking: KM

BOTTOM VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	0,5	A
Drain current (peak)	I_{DM}	max.	1,0	A
Total power dissipation up to $T_{amb} = 25\ ^oC$*	P_{tot}	max.	1	W
Storage temperature	T_{stg}		−65 to + 150	^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j\text{-}a}$	125	K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Drain-source breakdown voltage				
$I_D = 100\ \mu A$; $V_{GS} = 0$	$V_{(BR)DS}$	>	80	V
Drain-source leakage current				
$V_{DS} = 60\ V$; $V_{GS} = 0$	I_{DSS}	<	10	μA
Gate-source leakage current				
$V_{GS} = 20\ V$; $V_{DS} = 0$	I_{GSS}	<	100	nA
Gate threshold voltage		>	1,5	V
$I_D = 1\ mA$; $V_{DS} = V_{GS}$	$V_{GS(th)}$	<	3,5	V
Drain-source ON-resistance		typ.	2,0	Ω
$I_D = 500\ mA$; $V_{GS} = 10\ V$	R_{DSon}	<	4,0	Ω
Transfer admittance at f = 1 kHz				
$I_D = 500\ mA$; $V_{DS} = 15\ V$	$|Y_{fs}|$	typ.	300	mS
Input capacitance at f = 1 MHz		typ.	45	pF
→ $V_{DS} = 10\ V$; $V_{GS} = 0$	C_{is}	<	60	pF
Output capacitance at f = 1 MHz		typ.	30	pF
→ $V_{DS} = 10\ V$; $V_{GS} = 0$	C_{os}	<	45	pF
Feedback capacitance at f = 1 MHz		typ.	8	pF
→ $V_{DS} = 10\ V$; $V_{GS} = 0$	C_{rs}	<	12	pF
Switching times (see Figs 2 and 3)				
$I_D = 500\ mA$; $V_{DS} = 50\ V$; $V_{GS} = 0$ to 10 V	t_{on}	<	10	ns
	t_{off}	<	15	ns

* Transistors mounted on a substrate with surface area of 2,5 cm^2 and thickness of 0,7 mm.
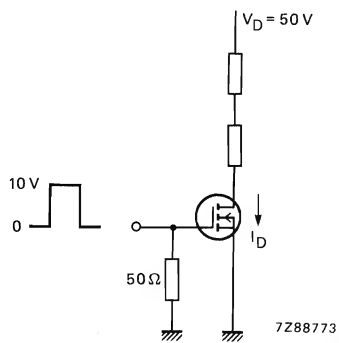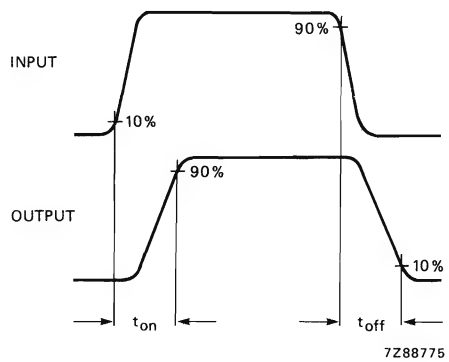
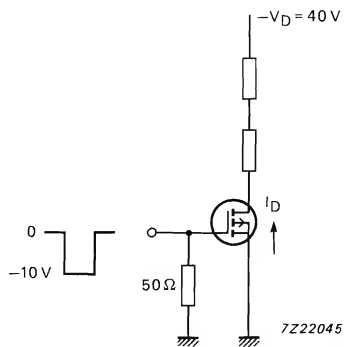Fig. 2 Switching times test circuit.

Fig. 3 Input and output waveforms.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in SOT-23 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for telephone ringer and for application with relay, high-speed and line transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	175	mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	300	mW
Drain-source ON-resistance $I_D = 150$ mA; $V_{GS} = 5$ V	R_{DSon}	typ. <	7 10	Ω Ω
Transfer admittance $I_D = 175$ mA; $V_{DS} = 5$ V; f = 1 kHz	$|Y_{fs}|$	typ.	150	mS

MECHANICAL DATA   Dimensions in mm

Fig. 1 SOT-23.

Marking: 02

TOP VIEW

7Z96885

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain surrent (d.c.)	I_D	max.	175	mA
Drain current (peak)	I_{DM}	max.	600	mA
Total power dissipation up to $T_{amb} = 25$ °C*	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}	−65 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified

Drain-source breakdown voltage $I_D = 100\ \mu A$; $V_{GS} = 0$	$V_{(BR)DS}$	>	80	V
Drain-source leakage current $V_{DS} = 60$ V; $V_{GS} = 0$	I_{DSS}	<	1,0	μA
Gate-source leakage current $V_{GS} = 20$ V; $V_{DS} = 0$	I_{GSS}	<	100	nA
Gate-source cut-off voltage $I_D = 1$ mA; $V_{DS} = V_{GS}$	$V_{(P)GS}$	> <	1,5 3,5	V V
Drain-source ON-resistance $I_D = 150$ mA; $V_{GS} = 5$ V	R_{DSon}	typ. <	7 10	Ω Ω
Transfer admittance at f = 1 kHz $I_D = 175$ mA; $V_{DS} = 5$ V	$|y_{fs}|$	typ.	150	mS
Input capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{is}	typ. <	15 30	pF pF
Output capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{os}	typ. <	13 20	pF pF
Feedback capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{rs}	typ. <	3 6	pF pF
Switching times (see Figs 2 and 3) $I_D = 175$ mA; $V_{DS} = 50$ V; $V_{GS} = 0$ to 10 V	t_{on}	typ. <	4 10	ns ns
	t_{off}	typ. <	4 10	ns ns

* Transistors mounted on a ceramic substrate of 7 mm x 5 mm x 0,7 mm.
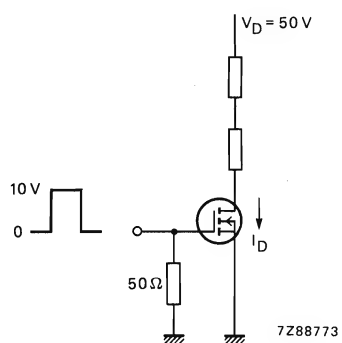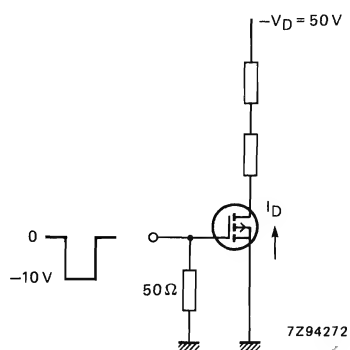
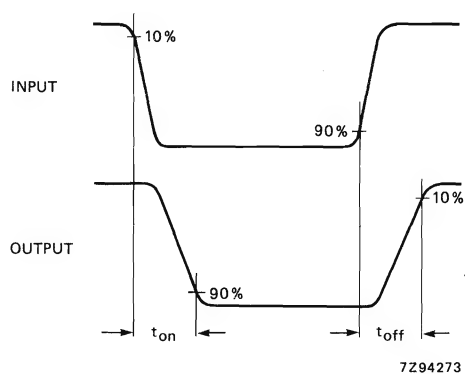Fig. 2 Switching times test circuit.
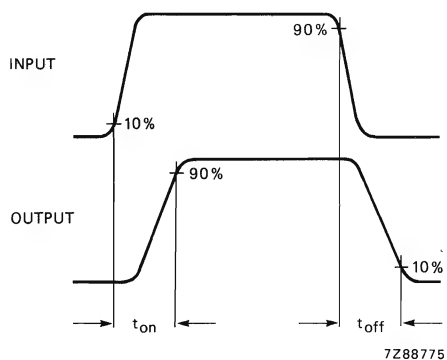
Fig. 3 Input and output waveforms.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel vertical D-MOS transistor in SOT-89 envelope and designed for use as line current inter-
rupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
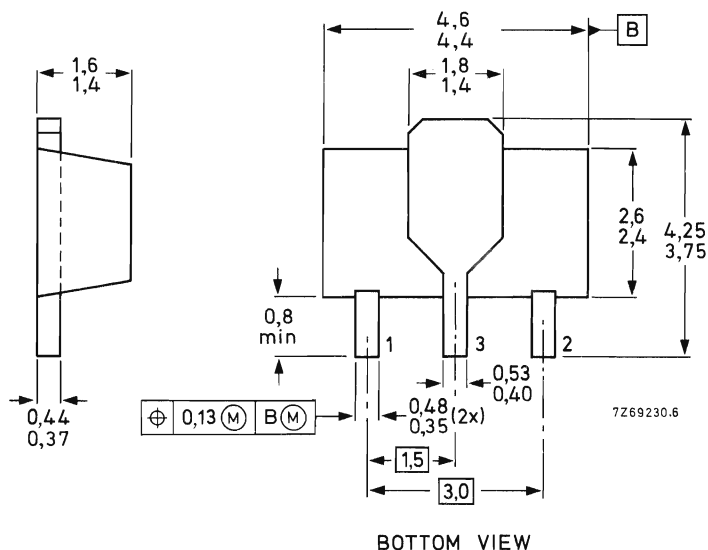- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	250	mA
Total power dissipation up to T_{amb} = 25 ^oC	P_{tot}	max.	1	W
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. <	6 12	Ω Ω
Transfer admittance I_D = 250 mA; V_{DS} = 15 V; f = 1 kHz	$\lvert y_{fs} \rvert$	typ.	250	mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-89.

Pinning:
1 = source
2 = gate
3 = drain

Marking: KN

BOTTOM VIEW

BST84

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	250	mA
Drain current (peak)	I_{DM}	max.	800	mA
Total power dissipation up to $T_{amb} = 25\ ^oC$*	P_{tot}	max.	1	W
Storage temperature	T_{stg}	−65 to + 150		^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	125	K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Drain-source breakdown voltage $I_D = 100\ \mu A; V_{GS} = 0$	$V_{(BR)DS}$	>	200	V
Drain-source leakage current $V_{DS} = 160\ V; V_{GS} = 0$	I_{DSS}	<	10	μA
Gate-source leakage current $V_{GS} = 20\ V; V_{DS} = 0$	I_{GSS}	<	100	nA
Gate threshold voltage $I_D = 1\ mA; V_{DS} = V_{GS}$	$V_{GS(th)}$	> <	0,8 2,8	V V
Drain-source ON-resistance $I_D = 250\ mA; V_{GS} = 10\ V$	R_{DSon}	typ. <	6 12	Ω Ω
Transfer admittance at $f = 1$ kHz $I_D = 250\ mA; V_{DS} = 15\ V$	$\|y_{fs}\|$	typ.	250	mS
Input capacitance at $f = 1$ MHz → $V_{DS} = 10\ V; V_{GS} = 0$	C_{is}	typ. <	70 90	pF pF
Output capacitance at $f = 1$ MHz → $V_{DS} = 10\ V; V_{GS} = 0$	C_{os}	typ. <	20 30	pF pF
Feedback capacitance at $f = 1$ MHz → $V_{DS} = 10\ V; V_{GS} = 0$	C_{rs}	typ. <	5 10	pF pF
Switching times (see Figs 2 and 3) → $I_D = 250\ mA; V_D = 50\ V; V_{GS} = 0$ to $10\ V$	t_{on}	typ. <	4 10	ns ns
	t_{off}	typ. <	15 25	ns ns

* Transistor mounted on a ceramic substrate with area of 2,5 cm² and thickness of 0,7 mm.
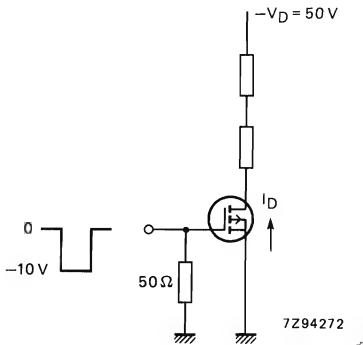
Fig. 2 Switching times test circuit.
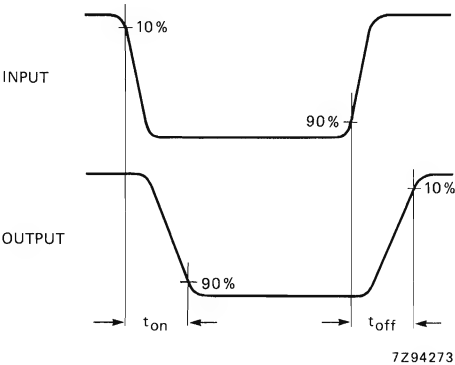

Fig. 3 Input and output waveforms.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in SOT-89 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for application with relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	180	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	200	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	300	mA
Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	1	W
Drain-source ON-resistance $I_D = 15$ mA; $V_{GS} = 3$ V	R_{DSon}	typ. $<$	7 10	Ω Ω
Transfer admittance $I_D = 300$ mA; $V_{DS} = 15$ V; $f = 1$ kHz	$|y_{fs}|$	typ.	250	mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-89.

Marking: K0

BOTTOM VIEW

7Z69230.6

BST86

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	180	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	200	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	300	mA
Drain current (peak)	I_{DM}	max.	800	mA
Total power dissipation up to $T_{amb} = 25$ °C*	P_{tot}	max.	1	W
Storage temperature	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j-a}$	=	125	K/W

CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified

Drain-source breakdown voltage $I_D = 100\ \mu A; V_{GS} = 0$	$V_{(BR)DS}$	>	180	V
Drain-source leakage current $V_{DS} = 120$ V; $V_{GS} = 0$	I_{DSS}	<	10	μA
Gate-source leakage current $V_{GS} = 20$ V; $V_{DS} = 0$	I_{GSS}	<	100	nA
Gate threshold voltage $I_D = 100\ \mu A; V_{DS} = V_{GS}$	$V_{GS(th)}$	> <	0,7 2,7	V V
Drain-source ON-resistance $I_D = 15$ mA; $V_{GS} = 3$ V	R_{DSon}	typ. <	7 10	Ω Ω
$I_D = 300$ mA; $V_{GS} = 10$ V	R_{DSon}	typ.	6	Ω
Transfer admittance at f = 1 kHz $I_D = 300$ mA; $V_{DS} = 15$ V	$|y_{fs}|$	typ.	250	mS
Input capacitance at f = 1 MHz → $V_{DS} = 10$ V; $V_{GS} = 0$	C_{is}	typ. <	50 65	pF pF
Output capacitance at f = 1 MHz → $V_{DS} = 10$ V; $V_{GS} = 0$	C_{os}	typ. <	20 30	pF pF
Feedback capacitance at f = 1 MHz → $V_{DS} = 10$ V; $V_{GS} = 0$	C_{rs}	typ. <	6 10	pF pF
Switching times (see Figs 2 and 3) $I_D = 300$ mA; $V_D = 50$ V; $V_{GS} = 0$ to 10 V	t_{on} t_{off}	< <	10 15	ns ns

* Transistors mounted on a ceramic substrate with area of 2,5 cm² and thickness of 0,7 mm.

Fig. 2 Switching times test circuit.

Fig. 3 Input and output waveforms.

DEVELOPMENT DATA

This data sheet contains advance information and
specifications are subject to change without notice.

BST95

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-39 envelope designed for application
in motor controls, power supplies etc.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	±20 V
Drain current (d.c.)	I_D	max.	2,0 A
Total power dissipation up to $T_C = 25\ {}^\circ C$	P_{tot}	max.	10 W
Drain-source on-state resistance $\quad I_D = 1,5\ A; V_{GS} = 10\ V$	$R_{DS(ON)}$	typ. <	1,8 Ω 2,0 Ω
Transfer admittance $\quad I_D = 1,5\ A; V_{DS} = 25\ V; f = 1\ kHz$	$|y_{fs}|$	typ.	0,8 S

MECHANICAL DATA
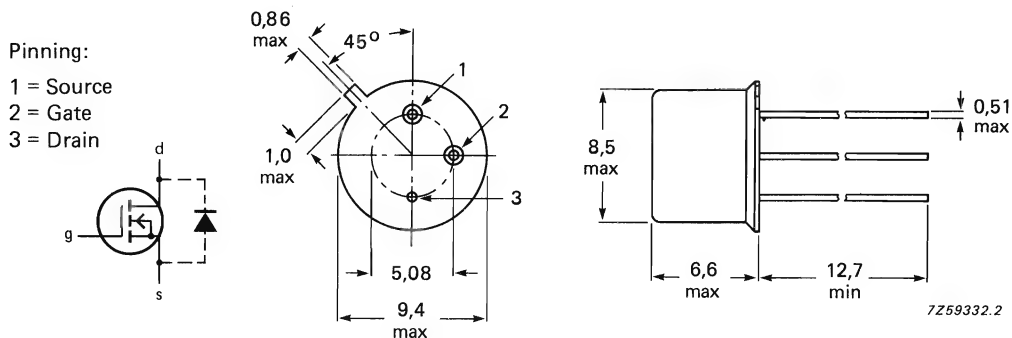
Dimensions in mm

Fig. 1 TO-39.

Pinning:

1 = Source
2 = Gate
3 = Drain

Accessories: 56245 (distance disc)

BST95

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	±20 V
Drain current (d.c.)	I_D	max.	2,0 A
Drain current (peak)	I_{DM}	max.	5,0 A
Total power dissipation up to T_C = 25 °C	P_{tot}	max.	10 W
Storage temperature range	T_{stg}		−65 to +150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to case	$R_{th\,j-c}$		12,5 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DS}$	>	200	V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	<	10	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	<	100	nA
Gate threshold voltage I_D = 1,0 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	> <	1,0 3,0	V V
Drain-source on-state resistance I_D = 1,5 A; V_{GS} = 10 V	$R_{DS(ON)}$	typ. <	1,8 2,0	Ω Ω
Transfer admittance at f = 1 kHz I_D = 1,5 A; V_{DS} = 25 V	$|y_{fs}|$	typ.	0,8	S
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ.	120	pF
Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ.	40	pF
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ.	9	pF
Switching times I_D = 1,5 A; V_D = 75 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	< <	35 50	ns ns
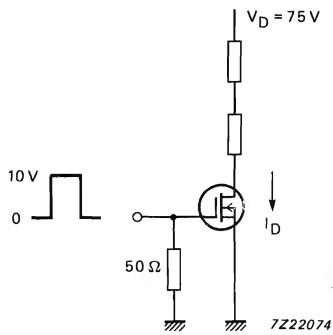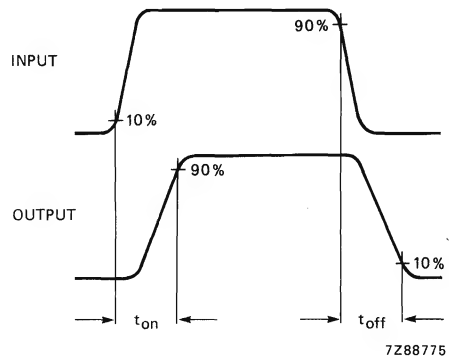
Fig. 2 Switching times test circuit.

Fig. 3 Input and output waveforms.

DEVELOPMENT DATA

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-18 and designed for use as line current interrupter in telephone sets and for application in relay, high speed and line transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	180	V
Drain-source voltage (non-repetitive peak; $t_p < 2$ ms)	$V_{DS(SM)}$	max.	200	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	300	mA
Total power dissipation up to $T_C = 25\ ^{o}C$	P_{tot}	max.	1,5	W
Drain-source ON-resistance $I_D = 300$ mA; $V_{GS} = 10$ V	R_{DSon}	typ.	6	Ω
Transfer admittance $I_D = 300$ mA; $V_{DS} = 15$ V; $f = 1$ kHz	$|y_{fs}|$	typ.	250	mS

MECHANICAL DATA   Dimensions in mm

Fig. 1 TO-18

7Z69420.1P

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	180	V
Drain-source voltage (non-repetitive peak; $t_p < 2$ ms)	$V_{DS(SM)}$	max.	200	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	300	mA
Drain current (peak)	I_{DM}	max.	800	mA
Total power dissipation up to $T_{amb} = 25\ ^{o}C$	P_{tot}	max.	0,4	W
Total power dissipation up to $T_C = 25\ ^{o}C$	P_{tot}	max.	1,5	W
Storage temperature	T_{stg}		-65 to $+150$	^{o}C
Junction temperature	T_j	max.	150	^{o}C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	310	K/W
From junction to case	$R_{th\ j-c}$	83	K/W

CHARACTERISTICS

$T_j = 25\ ^{o}C$ unless otherwise specified

Drain-source breakdown voltage $I_D = 100\ \mu A$; $V_{GS} = 0$	$V_{(BR)DS}$	$>$	180	V
Drain-source leakage current $V_{DS} = 120$ V; $V_{GS} = 0$	I_{DSS}	$<$	10	μA
Gate-source leakage current $V_{GS} = 20$ V; $V_{DS} = 0$	I_{GSS}	$<$	100	nA
Gate threshold voltage $I_D = 100\ \mu A$; $V_{DS} = V_{GS}$	$V_{GS(th)}$	$>$ $<$	0,7 2,7	V V
Drain-source ON-resistance (see Fig. 4) $I_D = 15$ mA; $V_{GS} = 3$ V	R_{DSon}	typ. $<$	7 10	Ω Ω
$I_D = 300$ mA; $V_{GS} = 10$ V	R_{DSon}	typ.	6	Ω
Transfer admittance at f = 1 kHz $I_D = 300$ mA; $V_{DS} = 15$ V	$|y_{fs}|$	typ.	250	mS
Input capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{is}	typ. $<$	50 60	pF pF
Output capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{os}	typ. $<$	20 30	pF pF
Feedback capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{rs}	typ. $<$	6 10	pF pF
Switching times (see Figs 2 and 3) $I_D = 300$ mA; $V_D = 50$ V; $V_{GS} = 0$ to 10 V	t_{on} t_{off}	$<$ $<$	10 15	ns ns

Fig. 2 Switching times test circuit.

Fig. 3 Input and output waveforms.

Fig. 4 $T_j = 25\ °C$; typ. values.

P-CHANNEL ENHANCEMENT MODE
VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features:

- Very low R_{DSon}
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	20	V
Drain current (d.c.)	$-I_D$	max.	0,3	A
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	1	W
Drain-source ON-resistance $-I_D = 200$ mA; $-V_{GS} = 10$ V	R_{DSon}	typ. max.	4,5 6	Ω Ω
Transfer admittance $-I_D = 200$ mA; $-V_{DS} = 15$ V; $f = 1$ kHz	$\lvert y_{fs}\rvert$	typ.	200	mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

diameter within 2,5 max
is uncontrolled

Note: Various pinnings are available on request.

BST100

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	20	V
Drain current (d.c.)	$-I_D$	max.	0,3	A
Drain current (peak)	$-I_{DM}$	max.	0,8	A
Total power dissipation up to $T_{amb} = 25\ ^oC*$	P_{tot}	max.	1	W
Storage temperature	T_{stg}	-65 to $+150$		^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j-a}$	125	K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Drain-source breakdown voltage $-I_D = 100\ \mu A; -V_{GS} = 0$	$-V_{(BR)DS}$	$>$	60	V
Drain-source leakage current $-V_{DS} = 45\ V; V_{GS} = 0$	$-I_{DSS}$	$<$	10	μA
Gate-source leakage current $-V_{GS} = 20\ V; V_{DS} = 0$	$-I_{GSS}$	$<$	100	nA
Gate threshold voltage $-I_D = 1\ mA; V_{DS} = V_{GS}$	$-V_{GS(th)}$	$>$ $<$	1,5 3,5	V V
Drain-source ON-resistance $-I_D = 200\ mA; -V_{GS} = 10\ V$	R_{DSon}	typ. $<$	4,5 6	Ω Ω
Transfer admittance at f = 1 kHz $-I_D = 200\ mA; -V_{DS} = 15\ V$	$\|y_{fs}\|$	typ.	200	mS
Input capacitance at f = 1 MHz $-V_{DS} = 10\ V; V_{GS} = 0$	C_{is}	typ. $<$	55 70	pF pF
Output capacitance at f = 1 MHz $-V_{DS} = 10\ V; V_{GS} = 0$	C_{os}	typ. $<$	30 45	pF pF
Feedback capacitance at f = 1 MHz $-V_{DS} = 10\ V; V_{GS} = 0$	C_{rs}	typ. $<$	8 12	pF pF
Switching times (see Figs 2 and 3) $-I_D = 200\ mA; -V_D = 50\ V; -V_{GS} = 0$ to 10 V	t_{on} t_{off}	typ. typ.	4 20	ns ns

* Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

Fig. 2 Switching times test circuit.

Fig. 3 Input and output waveforms.

P-CHANNEL VERTICAL D-MOS TRANSISTOR

P-channel enhancement mode D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Very low R_{DSon}
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	50	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	20	V
Drain current (d.c.)	$-I_D$	max.	0,25	A
Total power dissipation up to $T_{amb} = 25\ ^{\circ}C$	P_{tot}	max.	0,83	W
Drain-source ON-resistance $-I_D = 200$ mA; $-V_{GS} = 10$ V	R_{DSon}	typ. $<$	7,5 10	Ω Ω
Transfer admittance at f = 1 kHz $-I_D = 200$ mA; $-V_{DS} = 15$ V	$|y_{fs}|$	typ.	125	mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

diameter within 2,5 max is uncontrolled

Note: Various pinnings are available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	50	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	20	V
Drain current (d.c.)	$-I_D$	max.	0,25	A
Drain current (peak)	$-I_{DM}$	max.	0,5	A
Total power dissipation up to $T_{amb} = 25\ ^{\circ}C$*	P_{tot}	max.	0,83	W
Storage temperature	T_{stg}	-65 to $+150$		$^{\circ}C$
Junction temperature	T_j	max.	150	$^{\circ}C$

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j\text{-}a}$	=	150	K/W

CHARACTERISTICS

$T_j = 25\ ^{\circ}C$ unless otherwise specified

Drain-source breakdown voltage $-I_D = 100\ \mu A$; $V_{GS} = 0$	$-V_{(BR)DS}$	$>$	50	V
Drain-source leakage current $-V_{DS} = 40$ V; $V_{GS} = 0$	$-I_{DSS}$	$<$	10	μA
Gate-source leakage current $-V_{GS} = 20$ V; $V_{DS} = 0$	$-I_{GSS}$	$<$	100	nA
Gate threshold voltage $-I_D = 1$ mA; $V_{DS} = V_{GS}$	$-V_{GS(th)}$	$>$ $<$	1,5 3,5	V V
Drain-source ON-resistance $-I_D = 200$ mA; $-V_{GS} = 10$ V	R_{DSon}	typ. $<$	7,5 10	Ω Ω
Transfer admittance at f = 1 kHz $-I_D = 200$ mA; $-V_{DS} = 15$ V	$|y_{fs}|$	typ.	125	mS
Input capacitance at f = 1 MHz $-V_{DS} = 10$ V; $V_{GS} = 0$	C_{is}	typ.	30	pF
Output capacitance at f = 1 MHz $-V_{DS} = 10$ V; $V_{GS} = 0$	C_{os}	typ.	20	pF
Feedback capacitance at f = 1 MHz $-V_{DS} = 10$ V; $V_{GS} = 0$	C_{rs}	typ.	5	pF
Switching times (see Figs 2 and 3) $-I_D = 200$ mA; $-V_{DS} = 40$ V; $-V_{GS} = 0$ to 10 V	t_{on} t_{off}	typ. typ.	4 10	ns ns

* Transistor mounted on printed circuit board, max. lead length 4 mm.

Fig. 2 Switching times test circuit.

Fig. 3 Input and output waveforms.

P-CHANNEL VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in SOT-89 envelope and intended for use in relay, high-speed and line-transformer drivers, using SMD technology.

Features

- Very low R_{DSon}
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	20	V
Drain current (d.c.)	$-I_D$	max.	0,3	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance		typ.	4,5	Ω
$-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	max.	6	Ω
Transfer admittance				
$-I_D$ = 200 mA; $-V_{DS}$ = 15 V; f = 1 kHz	$\|y_{fs}\|$	typ.	200	mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-89.

Pinning:
1 = source
2 = gate
3 = drain

marking: LM

BOTTOM VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	20	V
Drain current (d.c.)	$-I_D$	max.	0,3	A
Drain current (peak)	$-I_{DM}$	max.	0,8	A
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	1	W
Storage temperature	T_{stg}	-65 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\,j\text{-}a}$	=	125	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 100 µA; $-V_{GS}$ = 0	$-V_{(BR)DS}$	>	60	V
Drain-source leakage current $-V_{DS}$ = 45 V; V_{GS} = 0	$-I_{DSS}$	<	10	µA
Gate-source leakage current $-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	100	nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	> <	1,5 3,5	V V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. <	4,5 6	Ω Ω
Transfer admittance at f = 1 kHz $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$|y_{fs}|$	typ.	200	mS
Input capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{is}	typ. <	55 70	pF pF
Output capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{os}	typ. <	30 45	pF pF
Feedback capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rs}	typ. <	8 12	pF pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_D$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on} t_{off}	typ. typ.	4 20	ns ns

* Transistor mounted on a ceramic substrate: area = 2,5 cm² and thickness = 0,7 mm.

Fig. 2 Switching time test circuit.

Fig. 3 Input and output waveforms.

DEVELOPMENT DATA

This data sheet contains advance information and
specifications are subject to change without notice.

BST122

P-CHANNEL VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in SOT-89 envelope and intended for use in relay, high-speed and
line-transformer drivers, using SMD-technology.

Features

- Very low R_{DSon}
- Direct interface to C-MOS, TTL
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	50	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	20	V
Drain current (d.c.)	$-I_D$	max.	0,25	A
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	1	W
Drain-source ON-resistance $-I_D = 200$ mA; $-V_{GS} = 10$ V	R_{DSon}	typ. max.	7,5 10	Ω Ω
Transfer admittance $-I_D = 200$ mA; $-V_{DS} = 15$ V; f = 1 kHz	$|y_{fs}|$	typ.	125	mS

MECHANICAL DATA   Dimensions in mm

Fig. 1 SOT-89.

Marking: LN

BOTTOM VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	50	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	20	V
Drain current (d.c.)	$-I_D$	max.	0,25	A
Drain current (peak)	$-I_{DM}$	max.	0,5	A
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	1	W
Storage temperature	T_{stg}	-65 to $+150$		^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j\text{-}a}$	$=$	125	K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Drain-source breakdown voltage				
$-I_D = 100\ \mu A; -V_{GS} = 0$	$-V_{(BR)DS}$	$>$	50	V
Drain-source leakage current				
$-V_{DS} = 1\ V; V_{GS} = 0$	$-I_{DSS}$	$<$	10	μA
Gate-source leakage current				
$-V_{GS} = 20\ V; V_{DS} = 0$	$-I_{GSS}$	$<$	100	nA
Gate threshold voltage				
$-I_D = 1\ mA; V_{DS} = V_{GS}$	$-V_{GS(th)}$	$>$	1,5	V
		$<$	3,5	V
Drain-source ON-resistance				
$-I_D = 200\ mA; -V_{GS} = 10\ V$	R_{DSon}	typ.	7,5	Ω
		$<$	10	Ω
Transfer admittance at f = 1 kHz				
$-I_D = 200\ mA; -V_{DS} = 15\ V$	$|y_{fs}|$	typ.	125	mS
Input capacitance at f = 1 MHz				
$\longrightarrow \quad -V_{DS} = 10\ V; V_{GS} = 0$	C_{is}	typ.	30	pF
		$<$	45	pF
Output capacitance at f = 1 MHz				
$\longrightarrow \quad -V_{DS} = 10\ V; V_{GS} = 0$	C_{os}	typ.	20	pF
		$<$	30	pF
Feedback capacitance at f = 1 MHz				
$\longrightarrow \quad -V_{DS} = 10\ V; V_{GS} = 0$	C_{rs}	typ.	5	pF
		$<$	10	pF
Switching times (see Figs 2 and 3)				
$\longrightarrow \quad -I_D = 200\ mA; -V_D = 50\ V; -V_{GS} = 0$ to $10\ V$	t_{on}	typ.	4	ns
	t_{off}	typ.	10	ns

* Transistor mounted on a ceramic substrate: area = 2,5 cm²; thickness = 0,7 mm.

Fig. 2 Switching times test circuit.

Fig. 3 Input and output waveforms.

DEVELOPMENT DATA

DEVELOPMENT DATA

This data sheet contains advance information and
specifications are subject to change without notice.

PH6659
PH6660
PH6661

N-CHANNEL VERTICAL D-MOS TRANSISTORS

N-channel enhancement mode vertical D-MOS transistors, in TO-92 variant envelopes and designed for application as low power, high-frequency inverters and line drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low $R_{DS(on)}$

QUICK REFERENCE DATA

			PH6659	PH6660	PH6661	
Drain-source voltage	V_{DS}	max.	35	60	90	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	20	20	V
Drain current (d.c.)	I_D	max.	0,75	0,5	0,5	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	1	1	W
Drain-source on-state resistance I_D = 1,0 A; V_{GS} = 10 V	$R_{DS(on)}$	typ. <	0,9 1,8	1,4 3,0	1,9 4,0	Ω Ω
Transfer admittance at f = 1 kHz I_D = 0,5 A; V_{DS} = 25 V	$|y_{fs}|$	>	170	170	170	mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant

Pinning:

1 = Drain
2 = Gate
3 = Source
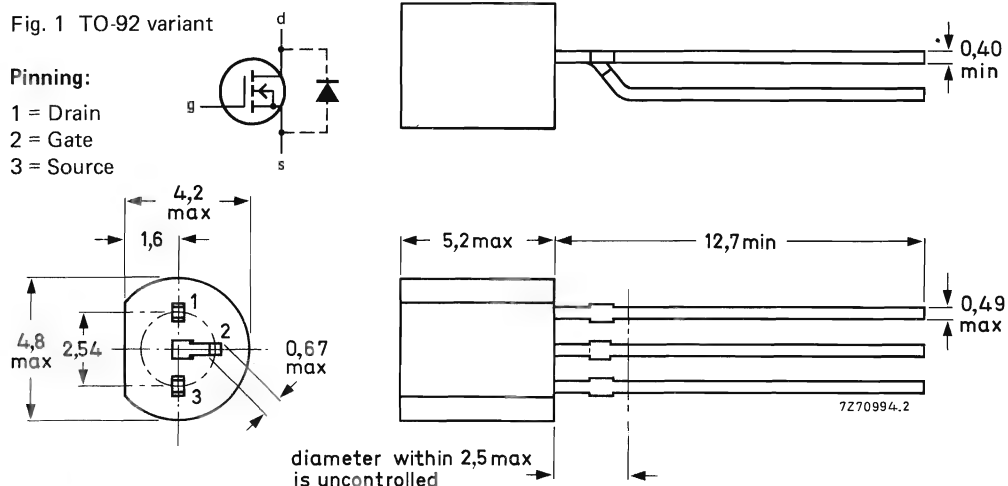
diameter within 2,5 max
is uncontrolled

7Z70994.2

Note: Various pinnings are available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			PH6659	PH6660	PH6661	
Drain-source voltage	V_{DS}	max.	35	60	90	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	20	20	V
Drain current (d.c.)	I_D	max.	0,75	0,5	0,5	A
Drain current (peak)	I_{DM}	max.		1,0		A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.		1		W
Storage temperature	T_{stg}			−65 to +150		°C
Junction temperature	T_j	max.		150		°C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j\text{-}a}$		125	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			PH6659	PH6660	PH6661	
Drain-source breakdown voltage I_D = 10 µA; V_{GS} = 0	$V_{(BR)DSS}$	>	35	60	90	V
Drain-source leakage current at V_{DS} = V_{DS} max; V_{GS} = 0	I_{DSS}	<	10	10	10	µA
Gate-source leakage current at V_{GS} = 15 V; V_{DS} = 0	I_{GSS}	<	100	100	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	> <	0,8 2,0	0,8 2,0	0,8 2,0	V V
On-state drain current V_{DS} = 25 V; V_{GS} = 10 V	$I_{D(ON)}$	> typ.	1,0 2,0	1,0 2,0	1,0 2,0	A A
Drain-source on-state resistance I_D = 0,3 A; V_{GS} = 5 V	$R_{DS(on)}$	typ. <	1,5 5,0	1,8 5,0	2,4 5,3	Ω Ω
I_D = 1,0 A; V_{GS} = 10 V	$R_{DS(ON)}$	typ. <	0,9 1,8	1,4 3,0	1,9 4,0	Ω Ω
Transfer admittance at f = 1 kHz I_D = 0,5 A; V_{DS} = 25 V	$|y_{fs}|$	>	170	170	170	mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	<	50	50	50	pF
Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	<	50	40	40	pF

* Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

N-channel vertical D-MOS transistor

			PH6659	PH6660	PH6661	
Feedback capacitance at f = 1 MHz						
V_{DS} = 25 V; V_{GS} = 0	C_{rss}	<	15	15	15	pF
Switching times						
I_D = 1,0 A; V_D = 25 V;	t_{on}	typ	5	5	5	ns
V_{GS} = 0 to 10 V		<	10	10	10	ns
	t_{off}	typ	5	5	5	ns
		<	10	10	10	ns

Fig. 2 Switching times test circuit.

Fig. 3 Input and output waveforms.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a TO-39 envelope and designed for application as low-power, high-frequency inverters and line drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low R_{DSon}

QUICK REFERENCE DATA

			2N6659	2N6660	2N6661	
Drain-source voltage	V_{DS}	max.	35	60	90	V
Gate-source voltage (open drain)	V_{GSO}	max.	30	30	30	V
Drain current (d.c.)	I_D	max.	1,4	1,1	0,9	A
Total power dissipation up to $T_c = 25\,^oC$	P_{tot}	max.	6,25	6,25	6,25	W
Drain-source ON-resistance $I_D = 1,0\,A; V_{GS} = 10\,V$	R_{DSon}	typ. $<$	0,9 1,8	1,4 3,0	1,9 4,0	Ω Ω
Transfer admittance at $f = 1\,kHz$ $I_D = 0,5\,A; V_{DS} = 25\,V$	$|y_{fs}|$	$>$	170	170	170	mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-39.
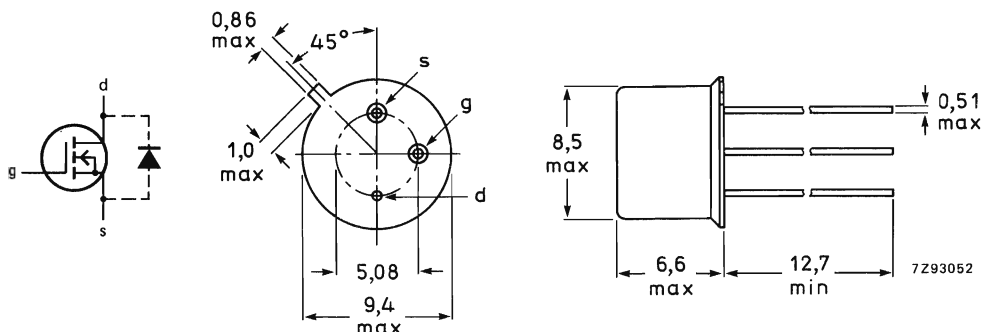
Maximum lead diameter is guaranteed only for 12,7 mm

Accessories: 56245 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			2N6659	2N6660	2N6661	
Drain-source voltage	V_{DS}	max.	35	60	90	V
→ Gate-source voltage (open drain)	V_{GSO}	max.	30	30	30	V
Drain current (d.c.)	I_D	max.	1,4	1,1	0,9	A
Drain current (peak)*	I_{DM}	max.		3,0		A
Total power dissipation up to T_c = 25 °C	P_{tot}	max.		6,25		W
Storage temperature	T_{stg}			−65 to + 150		°C
Junction temperature	T_j	max.		150		°C

THERMAL RESISTANCE

From junction to case	$R_{th\,j\text{-}c}$		20	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			2N6659	2N6660	2N6661	
Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	>	35	60	90	V
Drain-source leakage current at V_{DS} = V_{DSmax}; V_{GS} = 0	I_{DSS}	<	10	10	10	μA
Gate-source leakage current at V_{GS} = 15 V; V_{DS} = 0	I_{GSS}	<	100	100	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	> <	0,8 2,0	0,8 2,0	0,8 2,0	V V
ON-state drain current V_{DS} = 25 V; V_{GS} = 10 V	$I_{D(on)}$	> typ.	1,0 2,0	1,0 2,0	1,0 2,0	A A
Drain-source ON-resistance I_D = 0,3 A; V_{GS} = 5 V	R_{DSon}	typ. <	1,5 5,0	1,8 5,0	2,4 5,3	Ω Ω
I_D = 1,0 A; V_{GS} = 10 V	R_{DSon}	typ. <	0,9 1,8	1,4 3,0	1,9 4,0	Ω Ω
Transfer admittance at f = 1 kHz I_D = 0,5 A; V_{DS} = 25 V	$|y_{fs}|$	>	170	170	170	mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	<	50	50	50	pF
Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	<	50	40	40	pF

* Pulse conditions: $t_p \leqslant 300$ μs; δ = 0,01.

N-channel vertical D-MOS transistor

			2N6659	2N6660	2N6661	
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	$<$	15	15	15	pF
Switching times I_D = 1,0 A; V_D = 25 V; V_{GS} = 0 to 10 V	t_{on}	typ.	5	5	5	ns
		$<$	10	10	10	ns
	t_{off}	typ.	5	5	5	ns
		$<$	10	10	10	ns
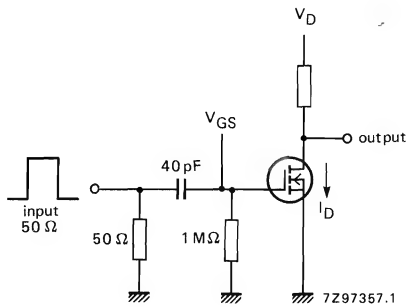
Fig. 2 Switching times test circuit.
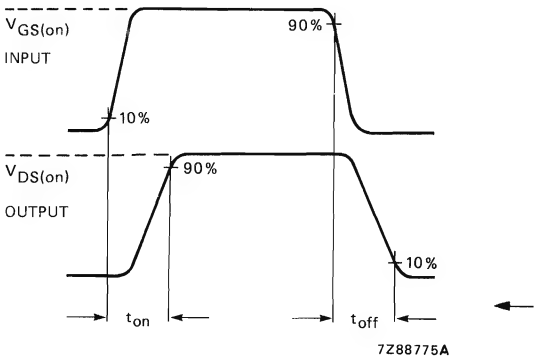
Fig. 3 Input and output waveforms.

MECHANICAL DATA   Dimensions in mm
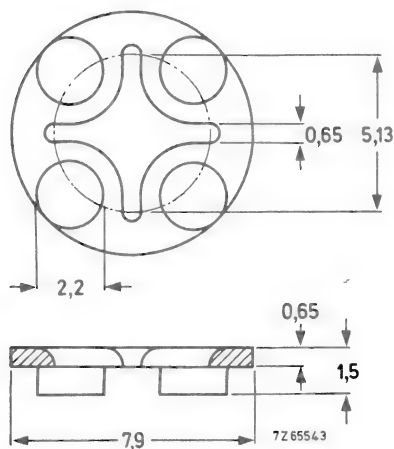
Distance disc 56245 for TO-5 or TO-39;
insulating material.
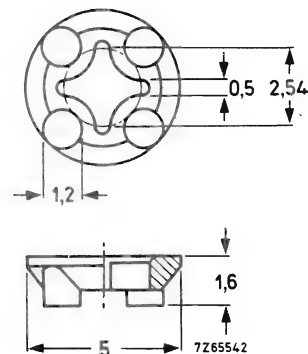
Distance disc 56246 for TO-18 or TO-72;
insulating material.

Maximum permissible temperature: 100 °C.

ROUND HEAD SCREW 6-32 UNC-2A

Available, upon request, under type number 56396 or 12 NC code number 9390 298 10xx0.

6-32 UNC-2A

12,7 (1/2 in)

7Z86986
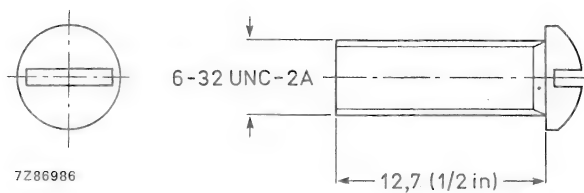
INDEX OF TYPE NUMBERS

The inclusion of a type number in this publication does not necessarily imply its availability.

Mm = Microminiature semiconductors for hybrid circuits
SD = Small-signal diodes
Sp = Special diodes
T = Tuner diodes
Vrg = Voltage regulator diodes

* = series
FET = Field-effect transistors
Mm = Microminiature semiconductors
    for hybrid circuits
P = Low-frequency power transistors
Sm = Small-signal transistors
T = Tuner diodes

P = Low-frequency power transistors

P = Low-frequency power transistors

FET = Field-effect transistors
HVP = High-voltage power transistors
Mm = Microniature semiconductors
     for hybrid circuits

P = Low-frequency power transistors
Sm = Small-signal transistors
WBT = Wideband transistors

*   = series
FET = Field-effect transistors
Mm = Microminiature semiconductors
         for hybrid circuits
RFP = R.F. power transistors and modules
RT   = Tripler

Sm   = Small-signal transistors
ThM = Thyristor modules
WBM = Wideband hybrid IC modules
WBT = Wideband transistors

*   = series
FET   = Field-effect transistors
RFP   = R.F. power transistors and modules

ThM = Thyristor modules
WBM = Wideband hybrid IC modules

FET = Field-effect transistors
Mm = Microminiature semiconductors
        for hybrid circuits
PDT = Photodiodes or transistors

RFP = R.F. power transistors and modules
Sm = Small-signal transistors
Th = Thyristors

* = series
FET = Field-effect transistors
Mm = Microminiature semiconductors
      for hybrid circuits
Sm = Small-signal transistors

SP = Low-frequency switching power transistors
Th = Thyristors
Tri = Triacs

* = series
PM = Power MOS transistors
R = Rectifier diodes
SP = Low-frequency switching power transistors

type no.	book	section	type no.	book	section	type no.	book	section
BY619	S1	R	BYV28*	S1/S2a	R	BYW96D	S1	R
BY620	S1	R	BYV29*	S2a	R	BYW96E	S1	R
BY627	S1	R	BYV29F*	S2a	R	BYX10G	S1	R
BY707	S1	R	BYV30*	S2a	R	BYX25*	S2a	R
BY708	S1	R	BYV31*	S2a	R	BYX30*	S2a	R
BY709	S1	R	BYV32*	S2a	R	BYX32*	S2a	R
BY710	S1	R	BYV32F*	S2a	R	BYX38*	S2a	R
BY711	S1	R	BYV33*	S2a	R	BYX39*	S2a	R
BY712	S1	R	BYV33F*	S2a	R	BYX42*	S2a	R
BY713	S1	R	BYV34*	S2a	R	BYX46*	S2a	R
BY714	S1	R	BYV36 *	S1	R	BYX50*	S2a	R
BYD13 *	S1	R	BYV39*	S2a	R	BYX52*	S2a	R
BYD14 *	S1	R	BYV42*	S2a	R	BYX56*	S2a	R
BYD17 *	S1/7	R	BYV43*	S2a	R	BYX90G	S1	R
BYD33 *	S1	R	BYV43F*	S2a	R	BYX96*	S2a	R
BYD37 *	S1/7	R	BYV44*	S2a	R	BYX97*	S2a	R
BYD73 *	S1	R	BYV60*	S2a	R	BYX98*	S2a	R
BYD74 *	S1	R	BYV72*	S2a	R	BYX99*	S2a	R
BYD77 *	S1	R	BYV73*	S2a	R	BZD23	S1	Vrg
BYM26 *	S1	R	BYV74*	S2a	R	BZD27	S1/7	Vrg
BYM36 *	S1	R	BYV79*	S2a	R	BZT03	S1	Vrg
BYM56 *	S1	R	BYV92*	S2a	R	BZV10	S1	Vrf
BYP21*	S2a	R	BYV95A	S1	R	BZV11	S1	Vrf
BYP22*	S2a	R	BYV95B	S1	R	BZV12	S1	Vrf
BYP59*	S2a	R	BYV95C	S1	R	BZV13	S1	Vrf
BYQ28*	S2a	R	BYV96D	S1	R	BZV14	S1	Vrf
BYR29*	S2a	R	BYV96E	S1	R	BZV37	S1	Vrf
BYR29F*	S2a	R	BYW25*	S2a	R	BZV46	S1	Vrg
BYT28*	S2a	R	BYW29*	S2a	R	BZV49*	S1/S7	Vrg/Mm
BYT79*	S2a	R	BYW29F*	S2a	R	BZV55*	S7	Mm
BYV10	S1	R	BYW30*	S2a	R	BZV80	S1	Vrf
BYV18*	S2a	R	BYW31*	S2a	R	BZV81	S1	Vrf
BYV19*	S2a	R	BYW54	S1	R	BZV85 *	S1	Vrg
BYV20*	S2a	R	BYW55	S1	R	BZW03 *	S1	Vrg
BYV21*	S2a	R	BYW56	S1	R	BZW14	S1	Vrg
BYV22*	S2a	R	BYW92*	S2a	R	BZW86*	S2a	TS
BYV23*	S2a	R	BYW93*	S2a	R	BZX55 *	S1	Vrg
BYV24*	S2a	R	BYW95A	S1	R	BZX70*	S2a	Vrg
BYV26 *	S1/S2a	R	BYW95B	S1	R	BZX75 *	S1	Vrg
BYV27*	S1/S2a	R	BYW95C	S1	R	BZX79*	S1	Vrg

```
*    = series
LED = Light-emitting diodes          PhC = Photocouplers
M    = Microwave transistors          R    = Rectifier diodes
Mm  = Microminiature semiconductors   TS  = Transient suppressor diodes
       for hybrid circuits            Vrf = Voltage reference diodes
Ph   = Photoconductive devices        Vrg = Voltage regulator diodes
```

*	= series			
A	= Accessories		M	= Microwave transistors
I	= Infrared devices		PhC	= Photocouplers
LED	= Light-emitting diodes		SEN	= Sensors

FET	= Field-effect transistors		R	= Rectifier diodes
I	= Infrared devices		SD	= Small-signal diodes
M	= Microwave transistors		SEN	= Sensors
Mm	= Microminiature semiconductors for hybrid circuits		Sm	= Small-signal transistors
			SP	= Low-frequency switching power transistors
P	= Low-frequency power transistors		St	= Rectifier stacks
PhC	= Photocouplers		WBM	= Wideband hybrid IC modules

```
*    = series
I    = Infrared devices
M    = Microwave transistors          R   = Rectifier diodes
P    = Low-frequency power transistors  SD  = Small-signal diodes
PhC  = Photocouplers                   Vrf = Voltage reference diodes
```

A   = Accessories
FET = Field-effect transistors
Ph = Photoconductive devices
PhC = Photocouplers
R   = Rectifier diodes

RFP = R.F. power transistors and modules
SD = Small-signal diodes
Sm = Small-signal transistors
WBT = Wideband transistors

A   = Accessories
FET = Field-effect transistors
Ph   = Photoconductive devices
PhC = Photocouplers
Sm   = Small-signal diodes

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DATA HANDBOOK SYSTEM

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

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SEMICONDUCTORS   RED

INTEGRATED CIRCUITS   PURPLE

COMPONENTS AND MATERIALS   GREEN

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T2b   **Transmitting tubes for communications, ceramic types**

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T4   **Magnetrons for microwave heating**

T5   **Cathode-ray tubes**
         Instrument tubes, monitor and display tubes, C.R. tubes for special applications

T6   **Geiger-Müller tubes**

T8   **Colour display systems**
         Colour TV picture tubes, colour data graphic display tube assemblies, deflection units

T9   **Photo and electron multipliers**

T10   **Plumbicon camera tubes and accessories**

T11   **Microwave semiconductors and components**

T12   **Vidicon and Newvicon camera tubes**

T13   **Image intensifiers and infrared detectors**

T15   **Dry reed switches**

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S2b   Thyristors and triacs

S3   Small-signal transistors

S4a   Low-frequency power transistors and hybrid modules

S4b   High-voltage and switching power transistors

S5   Field-effect transistors

S6   R.F. power transistors and modules

S7   Surface mounted semiconductors

S8a   Light-emitting diodes

S8b   Devices for optoelectronics
Optocouplers, photosensitive diodes and transistors, infrared light-emitting diodes and infrared sensitive devices, laser and fibre-optic components

S9   PowerMos transistors

S10   Wideband transistors and wideband hybrid IC modules

S11   Microwave transistors

S12   Surface acoustic wave devices

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             CMOS

IC05N   **HE4000B logic family — uncased ICs**
             CMOS

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             Logic family

IC08   **ECL 10K and 100K logic families**

IC09N   **TTL logic series**

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             Bipolar, MOS

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Small-signal field-effect transistors S5 1988